GCE A LEVEL MARKING SCHEME

SUMMER 2023

A LEVEL
ELECTRONICS – COMPONENT 2
A490U20-1

INTRODUCTION

This marking scheme was used by WJEC for the 2023 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

EDUQAS A LEVEL ELECTRONICS – COMPONENT 2

APPLICATION OF ELECTRONICS

SUMMER 2023 MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

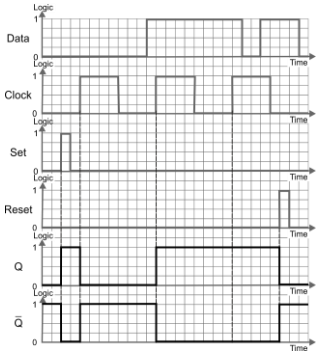
A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

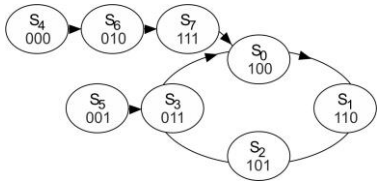
Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

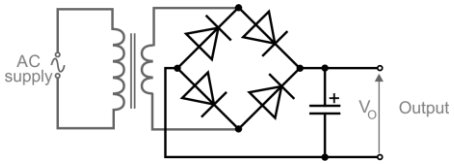
cao = correct answer only
ecf = error carried forward

<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="5">Marks available</th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>1</td><td>(a)</td><td></td><td>NOR, OR, XOR or XNOR gate [1]</td><td></td><td>1</td><td></td><td>1</td><td></td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>Using $f = 1.44 / (R_1 + 2R_2) C$
$f = 1.44 / (10 \times 10^3 + 2 \times 10 \times 10^3) 4.7 \times 10^{-6}$ [1]
$= 10.2$Hz [1]</td><td>1</td><td>1</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Using $T_{ON} / T_{OFF} = (R_1 + R_2) / R_2$
M:S ratio $= (10 \times 10^3 + 10 \times 10^3) / 10 \times 10^3$ [1]
$= 2:1$ [1]</td><td>1</td><td>1</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td>(c)</td><td></td><td>
<table>
<tr><th>C</th><th>B</th><th>A</th><th>P</th><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td></td><td colspan="3">Reset</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td></td><td colspan="3">Reset</td></tr>
</table>
One mark per correct ‘P’, ‘X’, ‘Y’, ‘Z’ column [4]
Reset correct [1]</td><td></td><td>4</td><td>1</td><td>5</td><td>5</td></tr>
<tr><td></td><td></td><td></td><td>Question 1 total</td><td>2</td><td>7</td><td>1</td><td>10</td><td>9</td></tr>
</table>

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	(a)		 Effect of Set [1] Effect of Reset [1] Effect of 1st clock pulse [1] Effect of 2nd and 3rd clock pulses [1] Q bar inverse of Q [1]	1	4		5	4
	(b)	(i)	$D_C = \underline{B} + \underline{C} \cdot \overline{\underline{A}}$ One mark per 'OR' term [2] $D_B = \overline{\underline{B}} + \overline{\underline{C}} \cdot \overline{\underline{A}}$ One mark per 'OR' term [2] $D_A = B \oplus A$ Correct logic expression [1]	1	4		5	4
		(ii)	<table><tr><th colspan="3">Current state</th><th colspan="3">Next state</th></tr><tr><th>C</th><th>B</th><th>A</th><th>D_C</th><th>D_B</th><th>D_A</th></tr><tr><td>1</td><td>0</td><td>0</td><td>**1**</td><td>**1**</td><td>**0**</td></tr><tr><td>1</td><td>1</td><td>0</td><td>**1**</td><td>**0**</td><td>**1**</td></tr><tr><td>1</td><td>0</td><td>1</td><td>**0**</td><td>**1**</td><td>**1**</td></tr><tr><td>0</td><td>1</td><td>1</td><td>**1**</td><td>**0**</td><td>**0**</td></tr><tr><td>0</td><td>0</td><td>0</td><td>**0**</td><td>**1**</td><td>**0**</td></tr><tr><td>0</td><td>0</td><td>1</td><td>**0**</td><td>**1**</td><td>**1**</td></tr><tr><td>0</td><td>1</td><td>0</td><td>**1**</td><td>**1**</td><td>**1**</td></tr><tr><td>1</td><td>1</td><td>1</td><td>**1**</td><td>**0**</td><td>**0**</td></tr></table> Main sequence correct [3] Unused states correct [1]	1	3		4	3

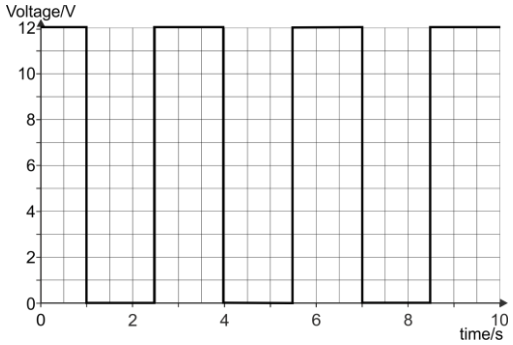
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(iii)	 Main sequence correct [1] Unused states correct [1] (Allow e.c.f. from (ii))	1	1		2	2
		(iv)	A stuck state is one which never leads into the main sequence. [1] If the system starts off in a stuck state, on power up, it will never progress into the **main sequence**. [1] (or equivalent answers)	2			2	
			Question 2 total	**6**	**12**	**0**	**18**	**13**

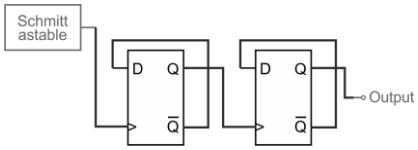
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	(a)		movlw b'10000000' One mark per instruction or operand [3] movwf TRISA	1	2		3	3
	(b)		begin clrf PORTA Instruction 1 mark; operand 1 mark [2] btfss PORTA,7 Instruction 1 mark; operand 1 mark [2] goto begin Instruction 1 mark [1] bsf PORTA,2 Operand 1 mark [1] call onesec call onesec Instruction 1 mark [1] call onesec Instruction 1 mark [1] goto begin Instruction 1 mark; operand 1 mark [2]	3	7		10	6
			Question 3 total	**4**	**9**	**0**	**13**	**9**

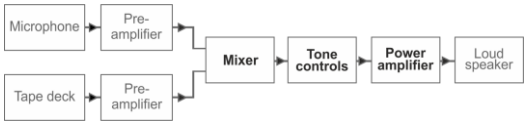
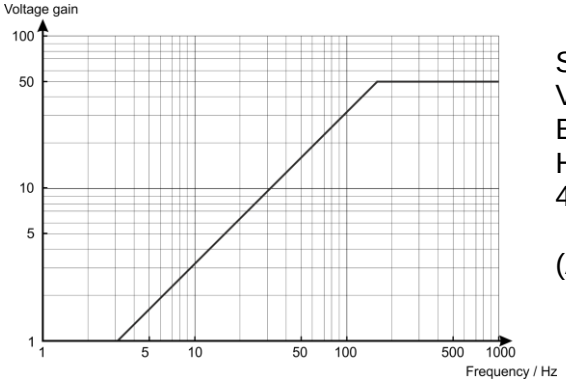
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
4	(a)		 4 diodes in bridge [1] Correct orientation [1] Smoothing capacitor correct [1]	2	1		3	
	(b)		Load regulation – output *voltage* steady *when output current changes.* Mention of output voltage [1] Mention of output current changing [1]	2			2	
	(c)	(i)	$V_L \approx V_Z(1 + R_F / R_1)$ gives $V_Z \approx V_L \times R_1 / (R_1 + R_F)$ Correct voltage [1] $V_Z = 15 \times 30 / (30 + 30)$ [1] $= 7.5V$ [1] Or solution such as: Op-amp maintains V_Z across lower 30kΩ resistor – 1 mark Identical voltage across upper resistor (same current) – 1 mark so $2 \times V_Z = 15V$ giving $V_Z = 7.5V$ – 1 mark (or equivalent)	1	2		3	1
		(ii)	$I_{OUT} = h_{FE} \times I_1$, ignoring currents into op-amp input and feedback chain $I_1 = I_{OUT} / h_{FE}$ [1] $= 320 / 40$ mA $= 8$mA [1]	1	1		2	2
		(iii)	Power dissipated in zener diode, P_Z = voltage V_Z across zener x current I_Z through zener I_Z = voltage across 100Ω resistor / 100Ω [1] $= (V_0 - V_Z) / 100 = (18 - 7.5) / 100 = 105$mA [1] $P_Z = 7.5 \times 1.05 = 787.5$mW (Accept 787.5 to 830mW) [1] (Allow e.c.f. from (c)(i))	1	2		3	2

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(iv)	When V_{OUT} falls, voltage fed back to op-amp inv. input falls. Then, difference between op-amp inputs increases, [1] causing op-amp output voltage to increase. [1] This pushes the output voltage back up again. [1]		3		3	
			Question 4 total	**7**	**9**	**0**	**16**	**5**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	(a)		**Indicative content:** **Power supply –** meets the spec. – works off a 6V battery. **Circuit** - is not wired correctly. Pin 6 should be connected to pin 7, not pin 2. **Activated by a push switch –** may meet the spec.– the switch must be pressed and released to provide a falling edge to trigger the monostable. **LED lights for one second if the light level is too low –** The capacitor value is incorrect. It should be 2.2μF, not nF. The series resistor is the correct value to protect the LED. **5-6 marks** A detailed analysis of the system is given. All factors identified above are evaluated accurately, using appropriate calculations. *There is a sustained line of reasoning which is coherent, relevant, substantiated and logically structured.* **3-4 marks** Most factors identified above, wrong power supply connections, wrong form of triggering, wrong value of capacitor, are evaluated accurately, supported by some calculation. *There is a line of reasoning which is partially coherent, largely relevant, supported by some evidence and with some structure.* **1-2 marks** The performance of the system is discussed in qualitative terms only. Two of the factors outlined above are evaluated correctly. *There is a basic line of reasoning which is not coherent, largely irrelevant, supported by limited evidence and with very little structure.* **0 marks** No attempt made or no response worthy of credit.			6	6	
			Question 5 total	**0**	**0**	**6**	**6**	**0**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	(a)		Time taken to charge from 0V to 6V (half of supply voltage) = half-life of RC network = 0.69RC. = 0.69 x 43 x 10^3 x 68 x 10^{-6} = 2.02s Correct populated formula [1] Answer [1] (or equivalent using charge formula)	1	1		2	1
	(b)	(i)	Using frequency f ≈ 1 / R C f = 1 / 43 x 10^3 x 68 x 10^{-6} = 0.34Hz Using period T = 1 / f T = 1 / 0.34 = 2.9s Populated frequency formula [1] Answer for frequency [1] Answer for period [1]	1	2		3	2
		(ii)	I V_C = 6V [1] II  Correct shape [1] Timing correct [1] Correct voltages [1] (Ignore M:S ratio)		4		4	4

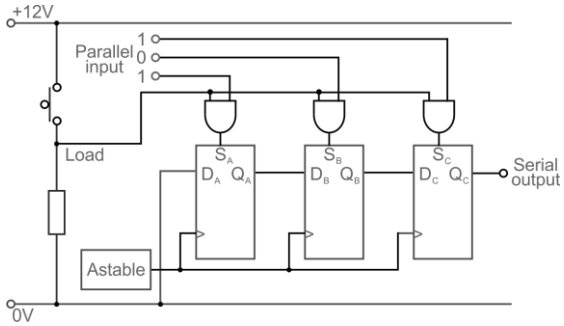
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(c)		 Use of 2 D-type flip-flops [1] Astable to 1st clock [1] Q bar to D twice [1] 2nd clock to 1st Q or Qbar [1] Output to 2nd Q or Q bar [1]			5	5	
			Question 6 total	**2**	**7**	**5**	**14**	**7**

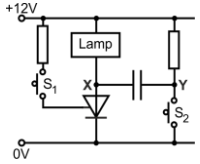
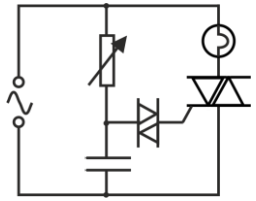
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7	(a)		 1 mark per correct answer [3]	3			3	
	(b)		Decoupling capacitors prevent DC signals affecting following block. (or equivalent) [1]	1			1	
	(c)	(i)	Active filters are those having a voltage gain >1. [1]	1			1	
		(ii)	Using voltage gain = $-R_F / R_{IN}$ [1] voltage gain = -750 / 15 = -50 [1] Using $f_b = 1 / 2 \Pi R C$ Use of 15kΩ resistor [1] $f_b = 1 / 2 \Pi 15 \times 10^3 68 \times 10^{-9}$ Multipliers [1] = 156Hz Answer [1]	1	4		5	3
		(iii)	 Shape of graph [1] Voltage gain [1] Break freq. [1] Horizontal gain [1] 45 degree roll-off [1] (Allow ecf from (c)(ii))	1	4		5	5

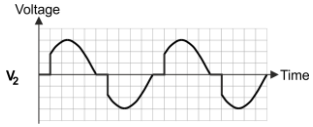
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(iv)	1st signal Amplitude = 3.75V Frequency = 300Hz 2nd signal Amplitude = 2.4V (±0.2V) Frequency = 100Hz (Allow e.c.f. from graph) Correct amplitudes – 1 mark each. Correct frequencies – 1 mark each [4] (Or by calculation)	1	3		4	3
			Question 7 total	**8**	**11**	**0**	**19**	**11**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8	(a)		Block A = ADC [1] Block B = PISO shift register [1] Block C = SIPO shift register [1] Block D = DAC [1]	4			4	
	(b)		Max. input signal = 5kHz [1] Equals half of the sampling gate frequency. [1] (or equivalent)	1	1		2	1
	(c)	(i)	Schmitt trigger regenerates signal, removing effects of noise and distortion. [1]	1			1	
		(ii)	Low-pass filter reduces unwanted high frequencies caused by quantisation. [1]	1			1	
	(d)	(i)	Pulse Amplitude Modulation (Accept PAM) [1]	1			1	
		(ii)	'X' positioned between sampling gate and block A (or between block D and low-pass filter.) [1]		1		1	
	(e)	(i)	FDM allocates a different carrier frequency to each signal. The signal is modulated onto the carrier and transmits continuously (within a limited frequency band centred on the carrier frequency). [1] In TDM, each signal source uses the full frequency bandwidth of the comms. link but only for a short time. Then a different source transmits in the same way, again for a limited time. In other words, the signal sources take turns to transmit down the comms. link. (or equivalent answers) [1]	2			2	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(ii)	PISO register generates 1 bit in $(2MHz)^{-1} = 0.5\mu s$ [1] PCM system produces 1 sample in $(10kHz)^{-1} = 100\mu s$ [1] Each sample contains 10 bits Hence each sample takes $10 \times 0.5 = 5\mu s$ to produce. [1] Gap between samples = $100\mu s$ so 20 such systems could use the comms. link. (or equivalent) [1]	1	3		4	4
			Question 8 total	**11**	**5**	**0**	**16**	**5**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9	(a)	(i)	Attenuation - cause such as impurities in the glass [1] (or scattering, connectors, splicing or equivalent.)	1			1	
		(ii)	Light pulse contains a number of frequencies. Each reflect at a slightly different angle resulting in the pulse spreading. [1]	1			1	
	(b)		Overall attenuation = 10 log P_{OUT} / P_{IN} = 10 log (5 x 10^{-6} / 100 x 10^{-6}) [1] = 10 log 1/20 = 13dB [1] Cable is 40km long so attenuation per km = 13 / 40 = 0.33dB/km [1]	1	2		3	2
	(c)		 Switch unit [1] Connection to logic gates [1] Parallel inputs to logic gates [1] Correct logic [1] Q to next D and output connected [1] Clock connections [1]			6	6	
	(d)		Photodiode operates in reverse bias, region **B** [1]	1			1	
			Question 9 total	**4**	**2**	**6**	**12**	**2**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
10	(a)	(i)	 S_1 connected correctly [1] Series resistor added [1]	2			2	
		(ii)	Voltage at **X** = 12V [1] Voltage at **Y** = 12V [1]		2		2	
		(iii)	Voltage at **X** = 0V [1] Voltage at **Y** = 12V [1]		2		2	
		(iv)	When S_2 is closed, voltage at Y falls by 12V to 0V so voltage at X must drop by around 12V to around -12V This reverse biases the thyristor, turning it and the lamp off. Description of voltages [1] Mention of reverse bias [1]	1	1		2	
	(b)	(i)	 RC network across power supply rails. [1] Correct connection to diac [1] Variable resistor used [1]	1	2		3	
		(ii)	Component P is a diac [1] Component Q is a triac [1]	2			2	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(iii)	I. Arrow V at peak of supply voltage V_S. [1] II.  'Off' periods correct [1] Shape [1]	2	1		3	2
			Question 10 total	**8**	**8**	**0**	**16**	**2**

GCE A LEVEL ELECTRONICS – COMPONENT 2

SUMMARY OF MARKS ALLOCATED TO ASSESSMENT OBJECTIVES

Question	AO1	AO2	AO3	TOTAL MARK	MATHS
1	2	7	1	**10**	9
2	6	12	0	**18**	13
3	4	9	0	**13**	9
4	7	9	0	**16**	5
5	0	0	6	**6**	0
6	2	7	5	**14**	7
7	8	11	0	**19**	11
8	11	5	0	**16**	5
9	4	2	6	**12**	2
10	8	8	0	**16**	2
TOTAL	**52**	**70**	**18**	**140**	**63**