GCE AS MARKING SCHEME

SUMMER 2024

AS
ELECTRONICS – COMPONENT 1
B490U10-1

About this marking scheme

The purpose of this marking scheme is to provide teachers, learners, and other interested parties, with an understanding of the assessment criteria used to assess this specific assessment.

This marking scheme reflects the criteria by which this assessment was marked in a live series and was finalised following detailed discussion at an examiners' conference. A team of qualified examiners were trained specifically in the application of this marking scheme. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners. It may not be possible, or appropriate, to capture every variation that a candidate may present in their responses within this marking scheme. However, during the training conference, examiners were guided in using their professional judgement to credit alternative valid responses as instructed by the document, and through reviewing exemplar responses.

Without the benefit of participation in the examiners' conference, teachers, learners and other users, may have different views on certain matters of detail or interpretation. Therefore, it is strongly recommended that this marking scheme is used alongside other guidance, such as published exemplar materials or Guidance for Teaching. This marking scheme is final and will not be changed, unless in the event that a clear error is identified, as it reflects the criteria used to assess candidate responses during the live series.

EDUQAS AS ELECTRONICS - COMPONENT 1
PRINCIPLES OF ELECTRONICS

SUMMER 2024 MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.
One tick must equate to one mark (except for the extended response question).
Question totals should be written in the box at the end of the question.
Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.
Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.
Crossed out responses not replaced should be marked.
Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

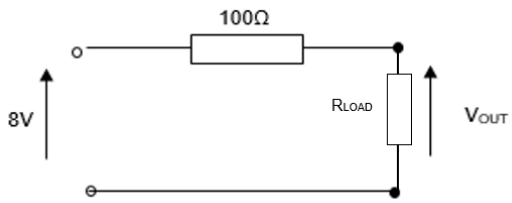
A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

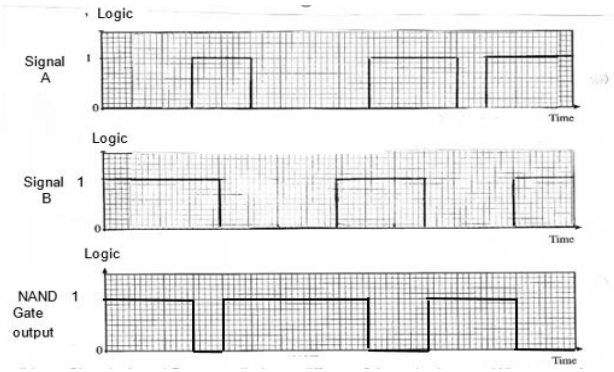
Marking abbreviations

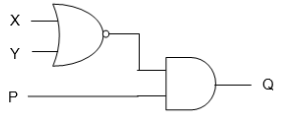
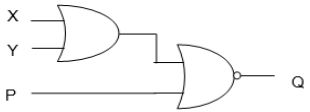
The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

cao = correct answer only
ecf = error carried forward

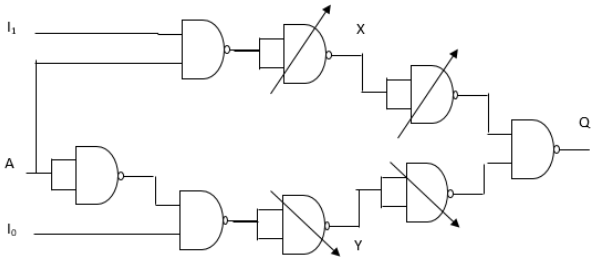
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
1.	*(a)*	(i)	300 x 0.017 = 5.1(V) (1)	1			1	1
		(ii)	12 - 5.1(ecf) = 6.9(V) (1) (can be implied) $\frac{6.9}{150}$ = 0.046(A) = 46m(A) (1)	1	 1		2	1
		(iii)	46 ecf from (ii) – 17 = 29 m(A) (1)	1			1	1
	(b)		P = 6.9 x 0.046 (1) (or 0.046^2 x 150) = 0.32(W) requirement NOT met (1) To award 2 marks 'Power rating NOT sufficient' must be seen.		1 1		2	1 1
	(c)	(i)	Substitution $V_{OC} = \frac{V_{IN}\ R_2}{R_1 + R_2} = \frac{12 \times 300}{150 + 300}$ (1) = 8(V) (1) Or use of $I = \frac{V_{IN}}{R_1 + R_2}$ and $V_{OC} = IR_2$ for 1st mark $I_{SC} = \frac{12}{150}$ = 0.08(A) (1) $R_0 = \frac{8}{0.08}$ = 100(Ω) (1) ecf on V_{OC}, I_{SC}	1	 1 1 1		 4	 4

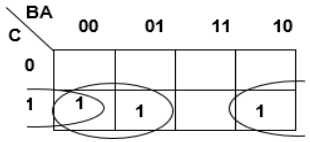
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(ii)	 R_{LOAD} added Correctly drawn equivalent circuit (1) All values labelled on the diagram - ecf from c(i) (1)	 1 1			 2	
		(iii)	V_{100} = 0.025 x 100 (ecf from c(i)) = 2.5(V) (1) V_{OUT} = 8 (ecf from c(i)) – 2.5 = 5.5(V) (1)	 1	1		2	1
			Question 1 total	**7**	**7**		**14**	**10**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2.	*(a)*		 Transitions in correct places (1) Logic levels correct (1)	1	1		2	
	(b)	(i)	To keep Y at logic 0 when switch B is open. (accept 'it acts as a pull-down resistor'/ to prevent short-circuit of the power rails)	1			1	
		(ii)	X = [logic] 1 Accept high / 5V	1			1	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(iii)	Inputs from switches to NOR gate Output of NOR and Pulses to AND gate Output of AND gate to Q  (Possible alternative OR then NOR)  Correct 3 gate solution 2 marks maximum X and Y through NOT gates and then to AND gate (max. 2)			1 1 1	3	
	(c)		$V_R = 5 - 2.3 = 2.7(V)$ (can be implied) (1) $R = \frac{2.7}{0.01} = 270(\Omega)$ (1)		1 1		2	1 1
			Question 2 total	**3**	**3**	**3**	**9**	**2**

<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="5">Marks available</th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>3.</td><td>(a)</td><td></td><td>X = I_1.A
Y = $I_0.\overline{A}$
Q = I_1.A + $I_0.\overline{A}$</td><td>1
1
1</td><td></td><td></td><td>3</td><td></td></tr>
<tr><td></td><td>(b)</td><td></td><td>
<table>
<tr><th>A</th><th>I_1</th><th>I_0</th><th>X</th><th>Y</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>
One mark each correct column (3)
ecf for column Q</td><td>3</td><td></td><td></td><td>3</td><td></td></tr>
</table>

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(c)	(i)	 NAND gate replacement of NOT correct (1) NAND gate replacement of OR correct (1) NAND gate replacement of AND correct x 2 (1)	3			3	
		(ii)	Two pairs (ecf) of gates identified and crossed out		2		2	
	(d)		A. $\overline{B}$+ $\overline{A}$. $\overline{B}$+ $\overline{A}$.B (1) **OR** $\overline{B}$(A + $\overline{A}$) + $(\overline{A + \overline{B}})$ (1) A. $\overline{B}$+ $\overline{A}$.($\overline{B}$+ B) (1) $\overline{B}$.1 +$\overline{A}$.B or $\overline{B}$ +$\overline{A}$.B (1 + 1) A. $\overline{B}$+ $\overline{A}$.1 (1) $\overline{B}$ + $\overline{A}$ or $\overline{B.A}$ (1) $\overline{B}$ + $\overline{A}$ or $\overline{B.A}$ (1) $\overline{A}$.B shown (1)		4		4	4
			Question 3 total	**9**	**6**	**0**	**15**	**4**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
4.	*(a)*		All $\bar{Q}$'s to D's (1) Pulses In to clock A then all $\overline{Q}$'s used to propagate signal (1) i.e.to subsequent clock inputs All Q's to output flags (1)	1 1 1			3	
	(b)	(i)	time = 4 x $\frac{1}{f}$ (= 40s) (1) or $\frac{1}{f}$ = 10 (s) No mark for answer 40 as this is given.		1		1	1
		(ii)	R = $\overline{C}$ (1) Y = B.A (1)	1	 1		2	
		(iii)	I. G = C.$\overline{B}$.$\overline{A}$ + C.$\overline{B}$.A + C.B.$\overline{A}$ (1) II.  Correct map (1) G = C.$\overline{B}$ + C.$\overline{A}$ (1 mark each correct term) Accept factorised version G = C. ($\overline{B}$ + $\overline{A}$) or C.$\overline{B.A}$		1 1 1 1		4	3

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		(iv)	R NOT gate between C and R (1) Y AND gate between A.B and Y (1) Then any one from: G1 NAND A with B then AND output with C G2 NOT A and NOT B to OR then AND output with C G3 NOT A and NOT B each to AND with C then both AND outputs to OR G4 Y (if correct) to NOT then AND with C G5 NOR R with Y G6 NOT R, NOT Y with AND	1 1 1			3	
	(c)	(i)	Any ONE from: Flexibility to make changes (such as timing): Fewer components. Simplified circuit design. (1)	1			1	
		(ii)	Is COUNT = 3 (1) (YES) Yellow LED ON (Red and Yellow ON and Green OFF) (1) Link from NO **with arrow** to just below Count = 0 box or to just above 10s delay (1)	1	1	1	3	
			Question 4 total	**9**	**7**	**1**	**17**	**4**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5.	*(a)*		P has 10s logic 1 pulse (1) starting from falling edge of T (1)… (2 to 12s) Q has 5s pulse between falling edge of P and rising edge of R (12 – 17s) (1)		1 1 1		3	
	(b)		To convert the **falling edge** of the monostable output to a **rising edge** in order to trigger the D-type flip-flop. (reference to both edges needed)		1		1	
	(c)	(i)	Resistor between 12V and pin 7 (1) Pin 7 and pin 6 connected (1) Capacitor between pin 6 and 0V (1)	1 1 1			3	
		(ii)	Select and use timing equation {T = 1.1 RC} $10 = 1.1 \times R \times 47 \times 10^{-6}$ (1) $R = \frac{9.1}{47 \times 10^{-6}}$ (1) R = 193 k(Ω) (1) Correct subs of T and C into a timing equation (1)		1 1 1		3	1 1 1
			Question 5 total	**3**	**7**	**0**	**10**	**3**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6.	*(a)*		Two diodes added in correct position and orientation to complete full-wave rectifier. (1) Connections to transformer and circuit completely correct (1) {Electrolytic} capacitor across output rails (1) Resistor labelled R across output rails (1)	1 1 1 1			4	
	(b)	(i)	$V_{OUT} = 12 - 1.4 = 10.6$ (V)		1		1	
		(ii)	$f_r = 100$ (Hz) (1)	1			1	
		(iii)	Select equation $V_r = \frac{I}{f_r C}$ (1) $V_r = \frac{0.4}{100 \times 1000 \times 10^{-6}}$ (1) $V_r = 4$ (V) (1) {ecf f_r from b(i)}	1	1 1		3	2
	(c)		Graph with 4 positive pulses (1) Voltage peaks at 10.6V ecf from b (i) (1) Graph shows ripple voltage (1) Magnitude of ripple voltage = 4(V) {ecf b (iii) } (1)	1 1 	 1 1		4	3
			Question 6 total	**8**	**5**	**0**	**13**	**5**

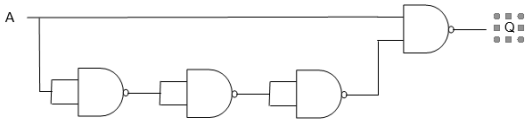
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7.	*(a)*		**Indicative Content:** **AO2 content:** applies knowledge transistor switching circuits and voltage dividers. **AO3 content:** analyses the circuit and uses appropriate calculations to determine whether or not the specification is met. Suggests any improvement(s) needed to fully meet the specification. **Method:** The voltage at X needs to be calculated using the transistor switch equations and separately using the voltage divider equation and the values compared. **Check $I_{pot\ div} \geq 10I_B$** As V_X calculated at 4°C is too low to saturate the transistor either the 560Ω resistor or the 4.3kΩ resistor must be reduced to an appropriate value **Calculations:** $I_B = 0.16/140 = 1.14$mA $V_R = 1.14 \times 4.3 = 4.9$ V $V_X = 4.9 + 0.7 = 5.6$ V Also $V_X = 12x400/(400 + 560) = 5$ V or reverse calculation. **Improvements:** Change 560Ω resistor: $5.6 = 12x400/(400 + R_{new})$ $R_{new} = 457\Omega$ (allow 457 or lower, preferred value not needed) **OR** Change 4.3kΩ resistor: 5 - 0.7 = 4.3 V 4.3/1.14 = 3.77 kΩ (allow 3.77kΩ or lower, preferred value not needed) **OR** Change transistor $V_X = 5$V therefore $I_B = 4.3/4.3 = 1.0$mA $h_{FE} = I_C/I_B = 160/1 = 160$	1	1	4	6	3

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			5-6 marks Comprehensive analysis of circuit performance measured against specification and supported by appropriate calculations of the voltage at X by both methods and comparison made. Conclusions drawn with reference to the evidence. *There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.* **3-4 marks** Voltage at X correctly calculated by either method or partial calculation attempted by both methods. Some comment on comparison between the behaviour of the circuit and the specification. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument.* **1-2 marks** Limited analysis with an attempt at least one calculation. *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.* **0 marks** *No attempt made or no response worthy of credit.*					

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(b)	(i)	Schmitt inverter (1)	1			1	
		(ii)	Correct re-arrangement $C = \frac{1}{fR}$ (1) substitution $C = \frac{1}{0.8 \times 560 \times 10^{3}}$ (1) $= 2.23\ \mu(F)$ (1)		1 1 1		3	3
			Question 7 total	**2**	**4**	**4**	**10**	**6**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8.	*(a)*	(i)	Feedback resistor R_F between output and inverting input (1) Input resistor R_1 between inverting input and 0V (1) Sensor connected to the non-inverting input (1) Resistor ratio 49:1 **and** both 1kΩ or greater (1) Resistors labelled correctly on the diagram (1) If correct inverting amplifier circuit drawn, 1st, 4th & 5th marks could be achieved.	1	1	3	5	1
	(b)	(i)	V_S = 12 x 8 (1) = 96 m(V) including matching unit (1)		1 1		2	2
		(ii)	Output voltage of amplifier $V_{OUT} = 50 \times V_S$ (1) = 4800 mV or 4.8V (1) ecf b(i)	1	 1		2	2
	(c)		$V_{IN}(max) = \frac{16}{50}$ (1) = 0.32 V = 320 mV (1) Max load = $\frac{320}{8}$ = 40 (kg) (1) $\frac{16}{8}$ (award 1)	1	 1 1		3	3
			Question 8 total	**3**	**6**	**3**	**12**	**8**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9.	*(a)*		Resistor and LDR (or other opto-electronic component) as potential divider at non-inverting input (1) Correct component orientation (LDR to 0V) (1) Diode connected across solenoid with correct orientation (1)	1 1 1			3	
	(b)		Allows the light level at which the system operated to be adjusted OR Reference voltage can be adjusted over range 0 – 15V (1)		1		1	
	(c)	(i)	Re-arranges and substitutes into formula $(V_{GS} -3) = \frac{I_D}{g_M} = \frac{6}{0.7}$ (1) $V_{GS} = 8.57 + 3 = 11.57$ (V) (1)	1	1		2	2
		(ii)	$P = I^2 r_{DS} = 36 \times 0.13$ (1) $= 4.68$ (W) (1) ecf on I_D of 30A from c (i).		1 1		2	2
	(d)		Any ONE from: Solenoid has high current and hence heating all night: Minor fluctuations of light at switching threshold can cause repeated switching.		1		1	
			Question 9 total	**4**	**5**	**0**	**9**	**4**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
10.	*(a)*		The time it takes the ***output*** of a logic gate to respond to a change in ***input***. (1)	1			1	
	(b)		Signal A connected to an input of a NAND gate in a correct propagation delay circuit (1) 3 NAND gates connected as NOT gates in series (1) Correct connections of NOT gates to circuit (1)  	1 1 1			3	
	(c)		Q remains at logic 1 / no change (1)		1		1	
			Question 10 total	**4**	**1**	**0**	**5**	**0**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
11.			**Indicative Content:** **Calculations:** There are a number of calculations required, in any order, leading to: Gain = -180 Bandwidth = 44.4kHz V_{OUT} =18V Slew-rate = 4.52 $V\mu s^{-1}$ if 18V is used; 3.8 $V\mu s^{-1}$ if 15V used. **Outcomes:** This means that the bandwidth of the amplifier is sufficient but there is clipping distortion and slew-rate distortion. **Solutions include:** increasing the power rail voltage to make saturation above 18V. Using an op-amp with a higher slew-rate. Solutions which involve reducing the amplitude and frequency of the test signal or changing the gain of the amp can get credit but not 6 marks. **Dealing with errors:** The evidence obtained by analysis must support candidates' conclusions. Where errors are made e.g. If the candidate used a test signal frequency of 4kHz by mistake this will reduce the calculated slew-rate and hence candidate must conclude there is no slew-rate distortion in order to gain credit.		1	5	6	4

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			5-6 marks Carries out most of the analysis above and compares calculated values with the specification identifying at least 2 of the 3 outcomes. Is able to suggest modifications where necessary to any identified fault. *There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.* **3-4 marks** Carries out some of the analysis above and compares calculated values with the specification identifying at least 1 of the 3 outcomes. Is able to suggest modifications where necessary to any identified fault. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument.* **1-2 marks** Carries out at least one relevant calculation and comments on the result is some meaningful way. *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.*					

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			0 marks *No attempt made or no response worthy of credit.*					
			Question 11 total		**1**	**5**	**6**	**4**
			TOTAL	**52**	**52**	**16**	**120**	**47**