GCE AS – NEW

B490U10-1

ELECTRONICS – AS component 1

Principles of Electronics

MONDAY, 21 MAY 2018 – MORNING

2 hours 30 minutes plus your additional time allowance

Surname _____

Other Names _____

Centre Number _____

Candidate Number 2 _____

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For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	5	
2.	8	
3.	15	
4.	9	
5.	10	
6.	16	
7.	10	
8.	5	
9.	17	
10.	13	
11.	12	
Total	120	

ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a DATA BOOKLET.

INSTRUCTIONS TO CANDIDATES

Use black ink, black ball-point pen or your usual method.

Answer ALL questions.

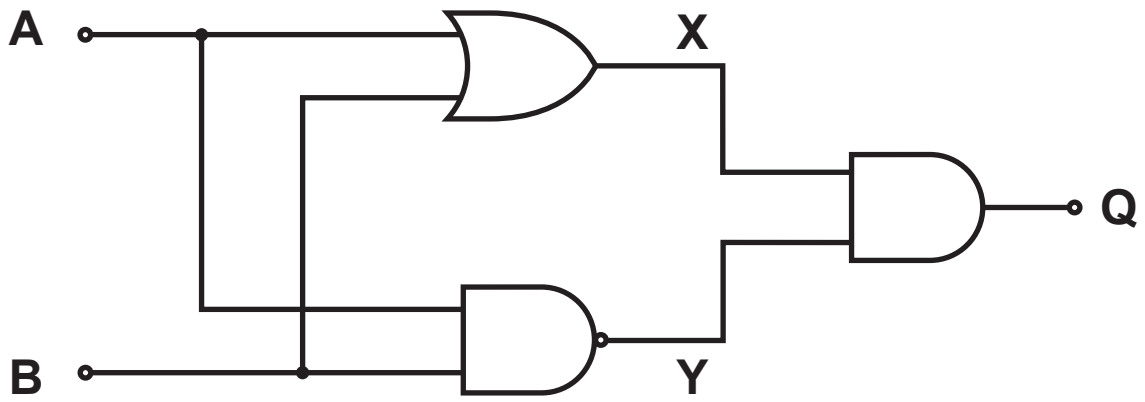
Write your name, centre number and candidate number in the spaces provided on the front cover.

Write your answers to all the questions in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

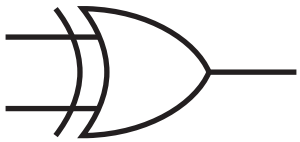
The assessment of the quality of extended response (QER) will take place in questions 5(a) and 11(b).



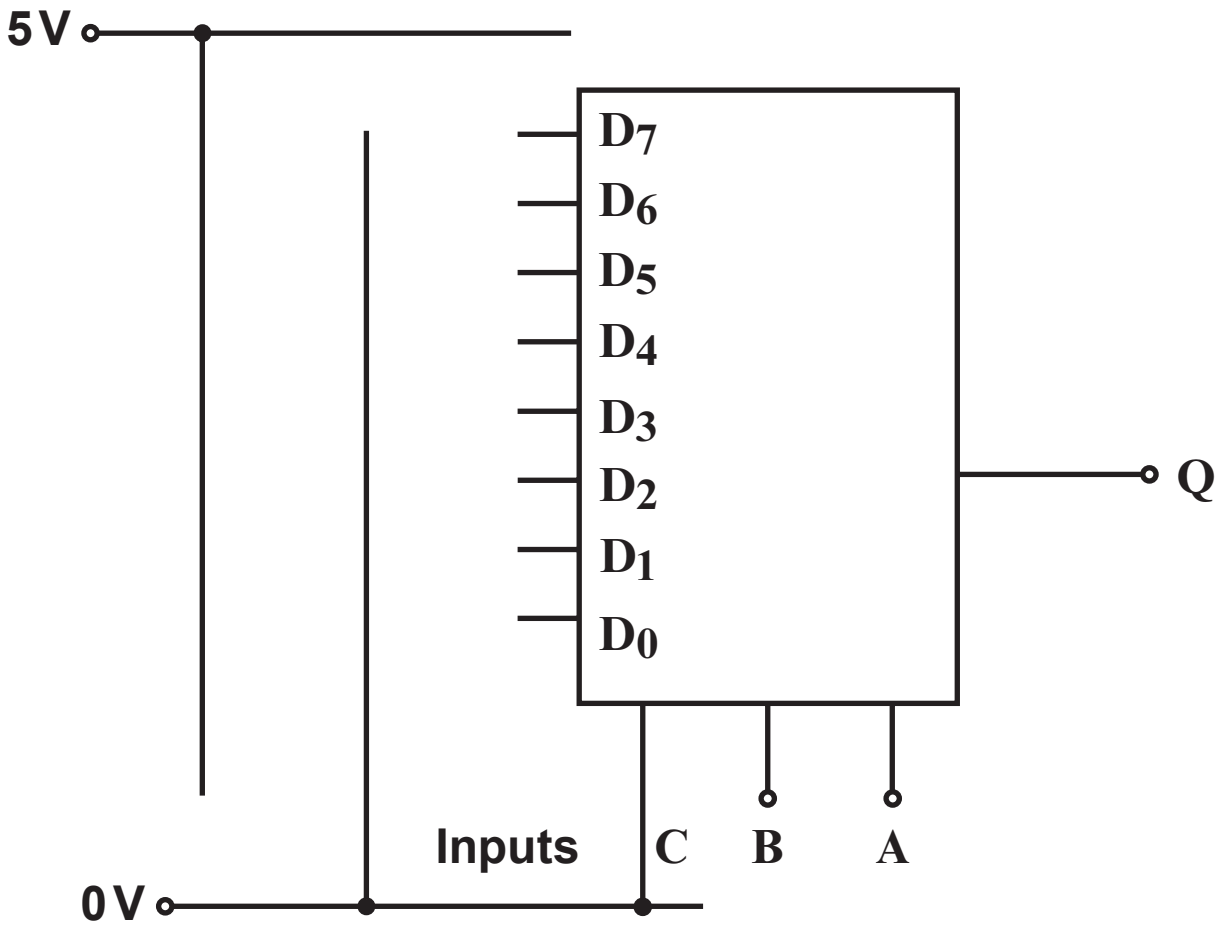
B	A	X	Y	Q
0	0			
0	1			
1	0			
1	1			

ANSWER ALL QUESTIONS.

1. The symbol for the 2-input EXOR gate is shown below.



(a) An EXOR gate can be built from other logic gates. Complete the truth table to show that the circuit opposite produces the same output as an EXOR gate. [3]


5 V
0 V
D7
D6
D5
D4
D3
D2
D1
D0
Q
Inputs
C
B
A

1(b) Multiplexers can be used in place of logic gates.

(i) Show on the diagram opposite how the output Q could be generated using a multiplexer. [1]

(ii) State ONE advantage of using a multiplexer for this purpose. [1]

_____

_____

_____

_____

2(a) Simplify the following expressions. [2]

(i) $\overline{B}$ **.0** _____

(ii) **A.B +** $\overline{B}$ **=** _____

(b) A logic system produced the following Karnaugh map.

DC \ BA	00	01	11	10
00	1	1	0	0
01	1	0	1	1
11	0	0	1	1
10	1	1	0	0

On the map show all the groups. Hence give the simplest Boolean expression for the output of this logic system. [3]

_____

_____

_____

2(c) Apply DeMorgan's theorem to the following expression AND simplify the result. [3]

$$Q = \overline{(\overline{A} + B)} + \overline{A}$$

Door switch C	Seatbelt switch B	Key sensor A	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

3. A design brief for an electronic safety warning system in a car uses the following information regarding the inputs and outputs of the system.

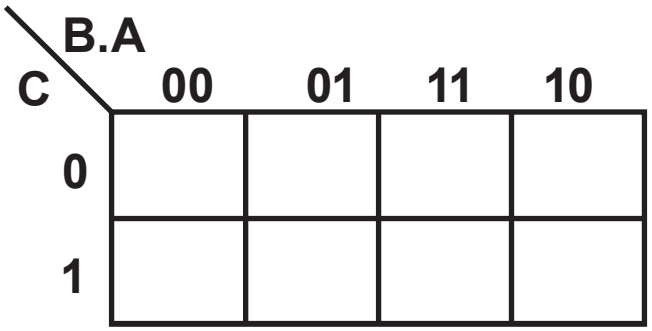
- sensor, A, outputs a logic 1 when the ignition key is turned.
- microswitch, B, on the seatbelt outputs a logic 1 when the belt is fastened.
- microswitch, C, on the door outputs a logic 1 if the door is opened.
- the buzzer sounds when Q is logic 1.

The truth table for the logic system is shown opposite.

(a) (i) Use the truth table to write down the UNSIMPLIFIED (3 term) Boolean expression for output Q in terms of C, B and A. [1]

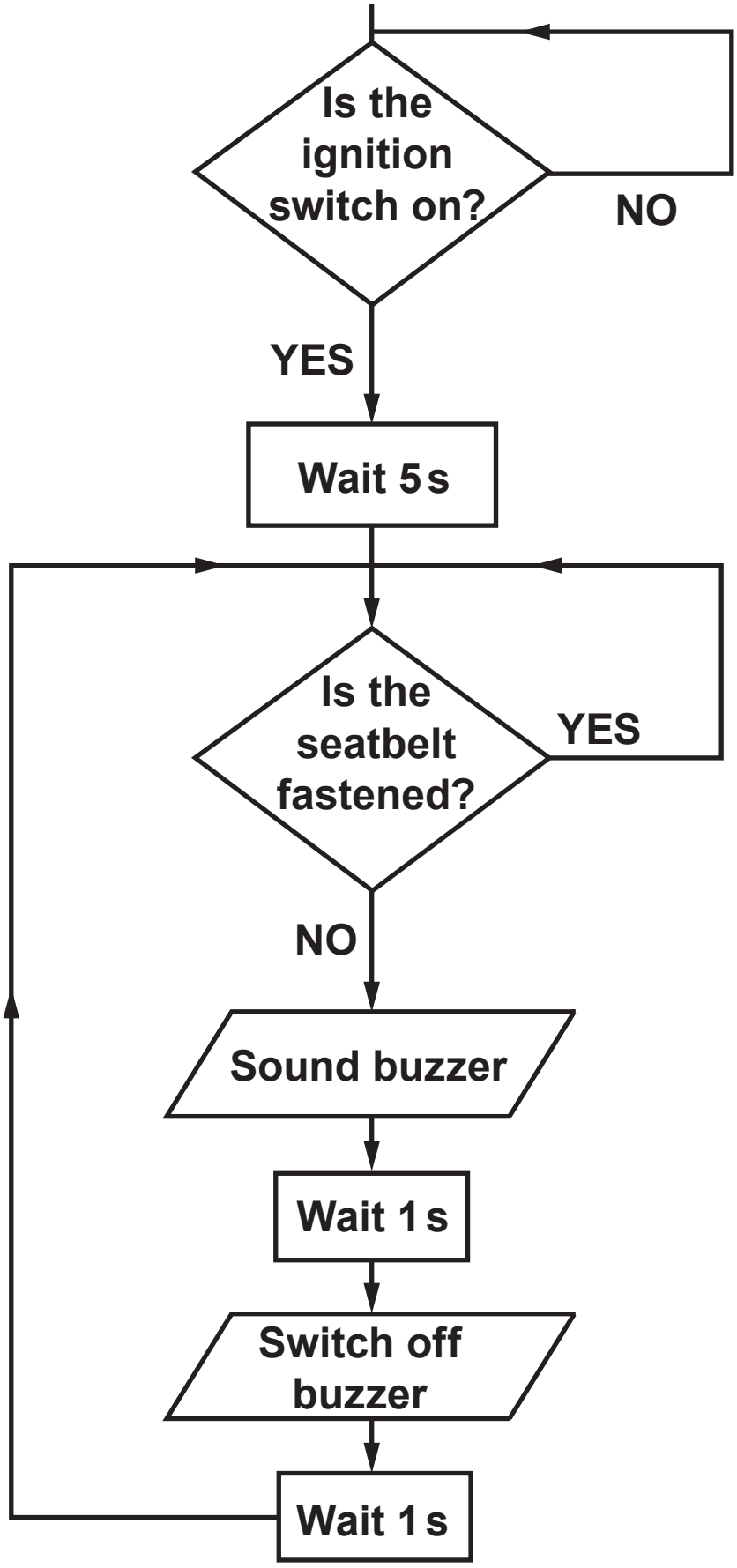
Q = _____

3(a) (ii) Simplify the expression using either a Karnaugh map or the rules of Boolean algebra. [3]



3(b) Complete the following diagram to show how the output Q can be generated using logic gates. [3]

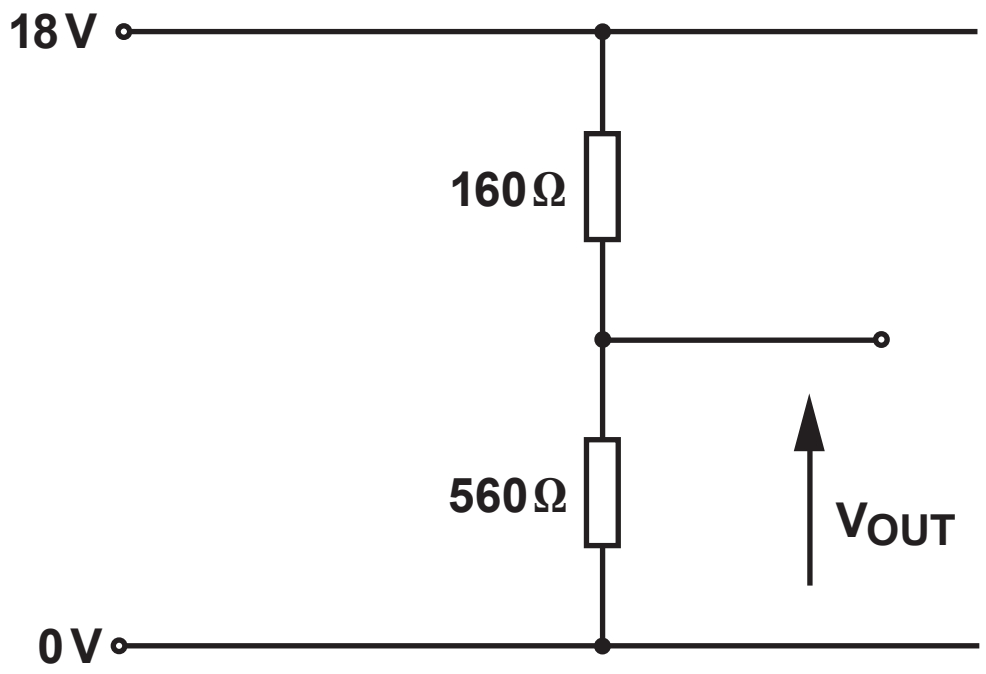
3(c) Redraw the system using NAND gates only. Cross out any redundant gates. [4]


Is the ignition switch on?
NO
YES
Wait 5 s
Is the seatbelt fastened?
YES
NO
Sound buzzer
Wait 1 s
Switch off buzzer
Wait 1 s

3(d) The system is replaced by a microcontroller. Part of the system is shown in the flow chart. Explain what is happening whilst the flow chart is run. [4]

13

4. The following circuit is used as a voltage source.

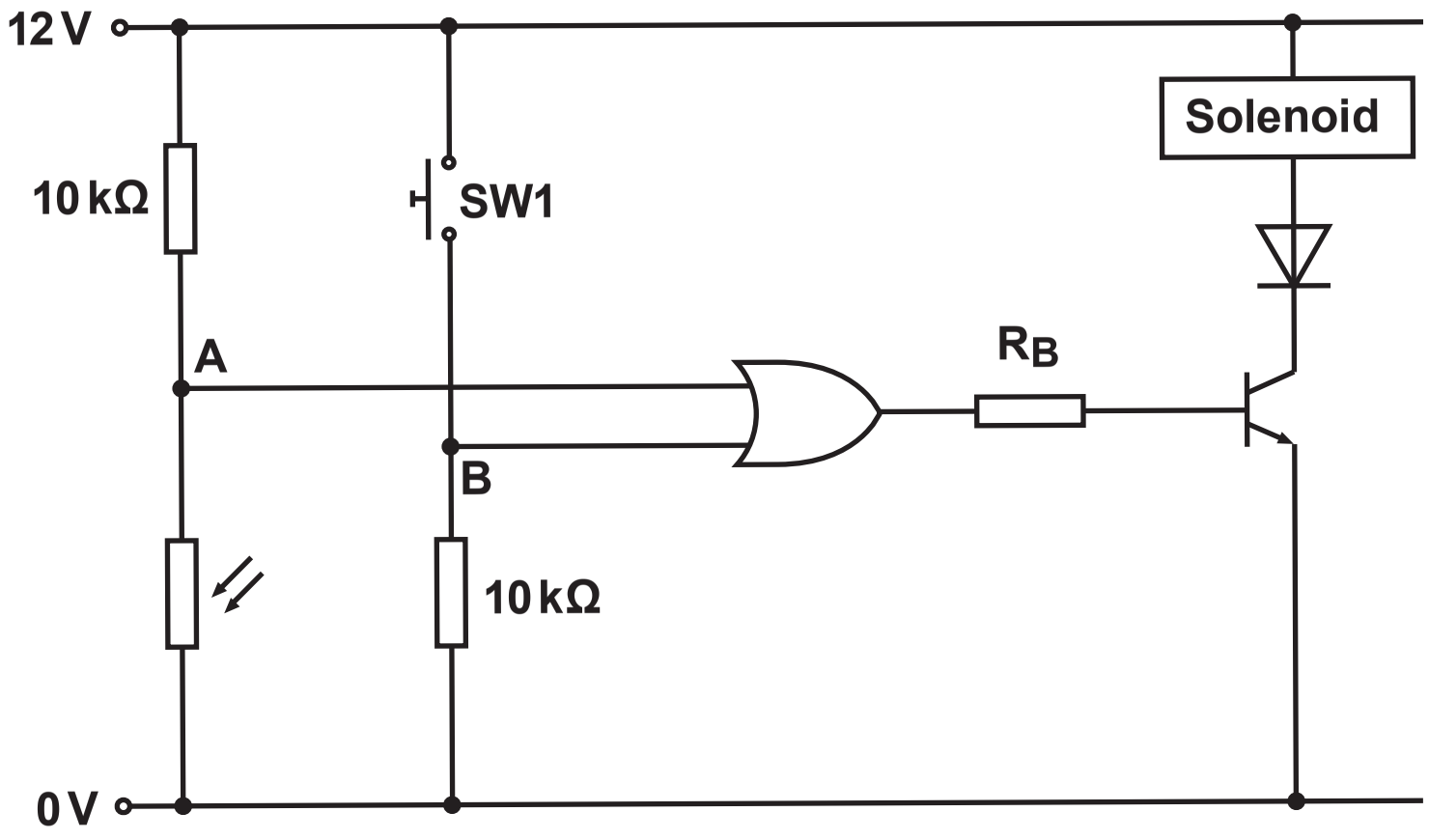


(a) Thevenin's theorem is used to produce an equivalent circuit.
Calculate the open circuit voltage V_{OC} and the equivalent resistance R_O. [4]

4(b) (i) **Draw the labelled equivalent circuit with two 240 Ω resistors connected in parallel across the output terminals. [2]**

4(b) (ii) Use the equivalent circuit to calculate the voltage drop across the output terminals.

[3]


12 V
10 kΩ
SW1
Solenoid
A
R_B
B
10 kΩ
0 V

5. **An electronic control system has the following circuit specification:**

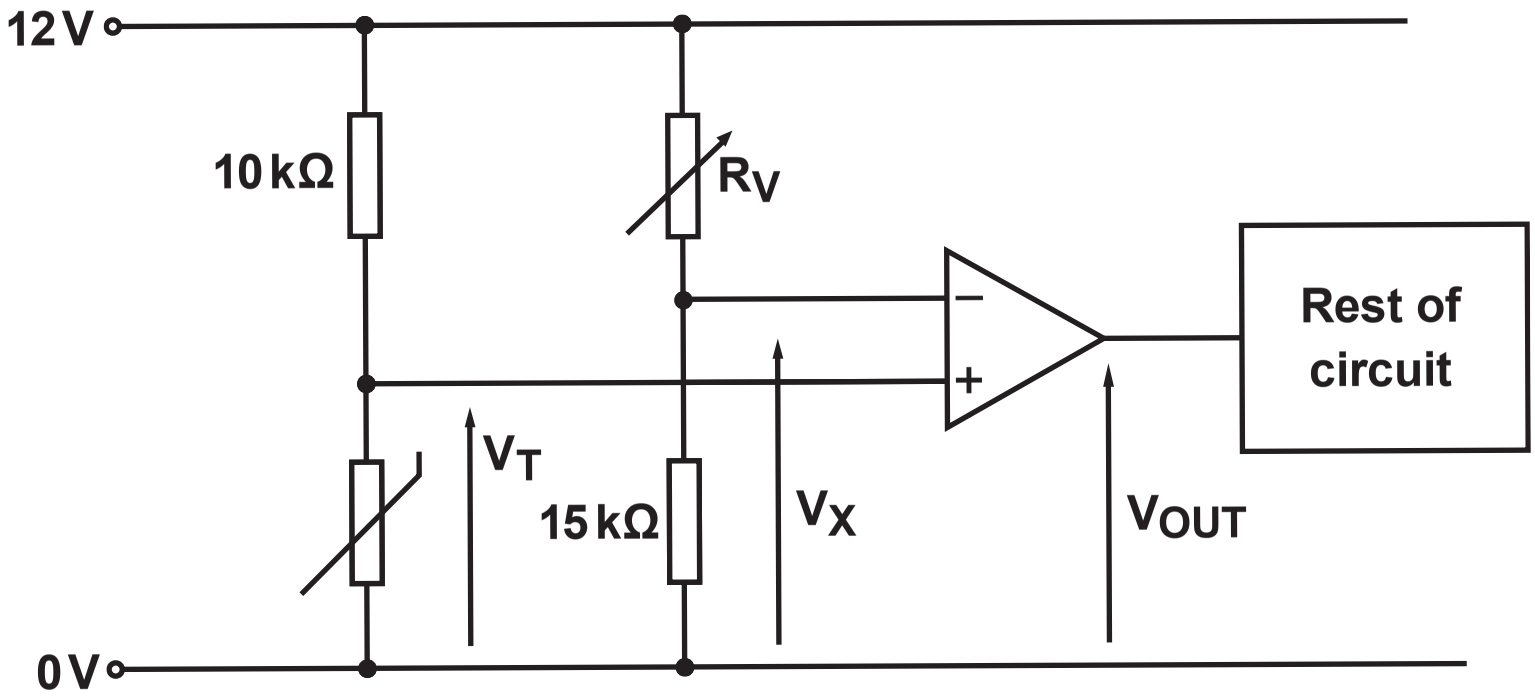
- **a solenoid should operate when either a light beam is broken or a switch is pressed**
- **when the light beam is broken point A should be at logic 1**
- **when the switch SW1 is pressed point B should be at logic 1**
- **a diode is required to protect the transistor from back emf.**

A design for the system is shown opposite.

(a) **Evaluate the function of the design shown in the diagram against the circuit specification and suggest any improvements required to meet the specification fully. [6 QER]**

5(b) (i) **The logic system output is 11.6 V and the current through the solenoid is 200 mA when the transistor is JUST SATURATED. The transistor has a current gain, h_{FE}, of 80.**
Calculate the ideal value for base resistor, R_B. [3]

(ii) **Choose a suitable preferred value resistor from the E24 series. [1]**



V_{OUT} saturates at 12 V and 0 V.

6. **A student designs a control system to keep the temperature of a tropical fish tank at 25°C. The circuit diagram opposite shows part of the control system.**

(a) (i) **Use the resistance-temperature graph to determine the resistance of the thermistor (R_T) at 25 °C and hence calculate the value of V_T at this temperature. [3]**

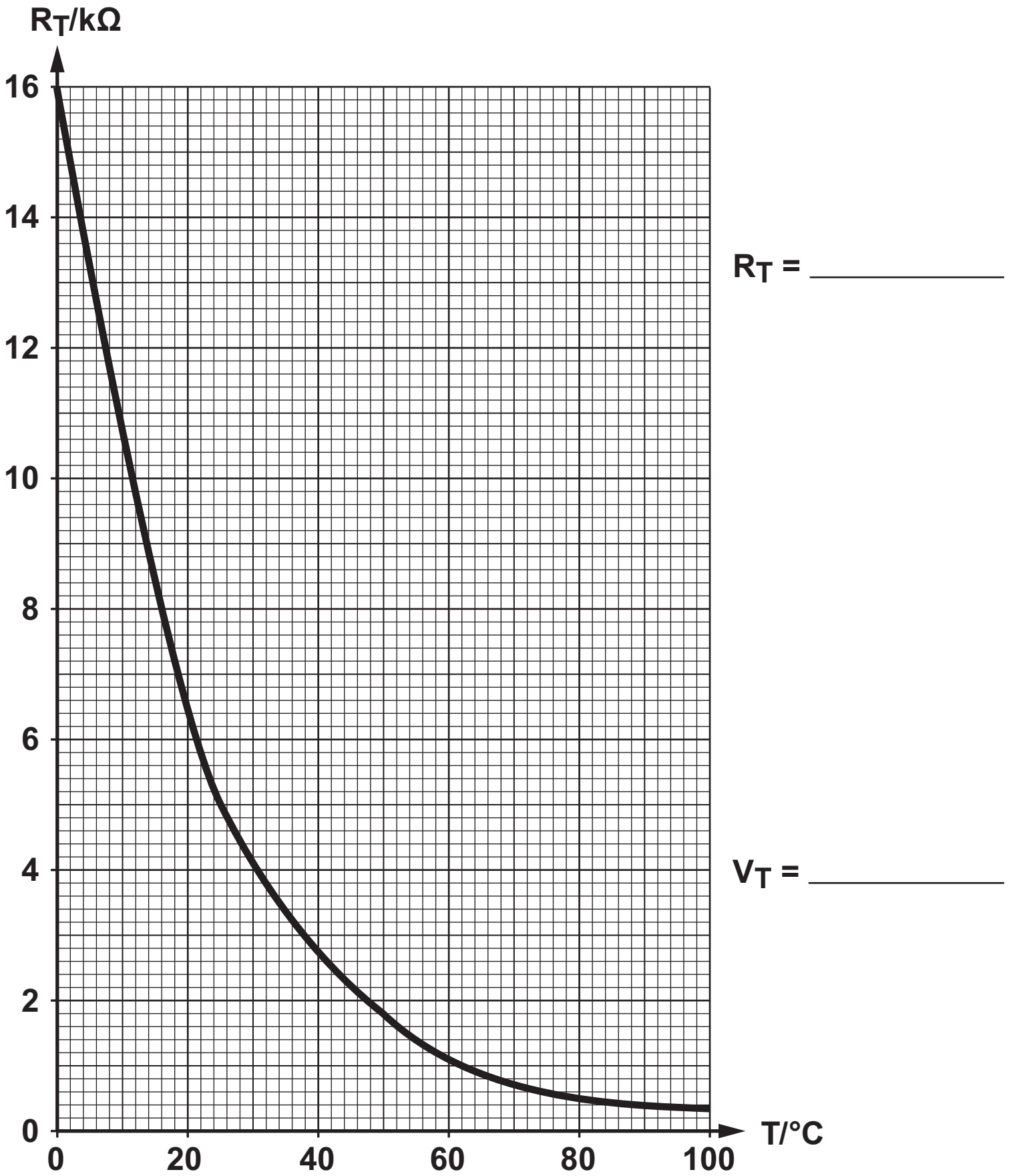
(ii) **Calculate the resistance of R_V that would cause the output voltage of the comparator to switch at just over 25 °C. [2]**

_____

_____

_____

_____

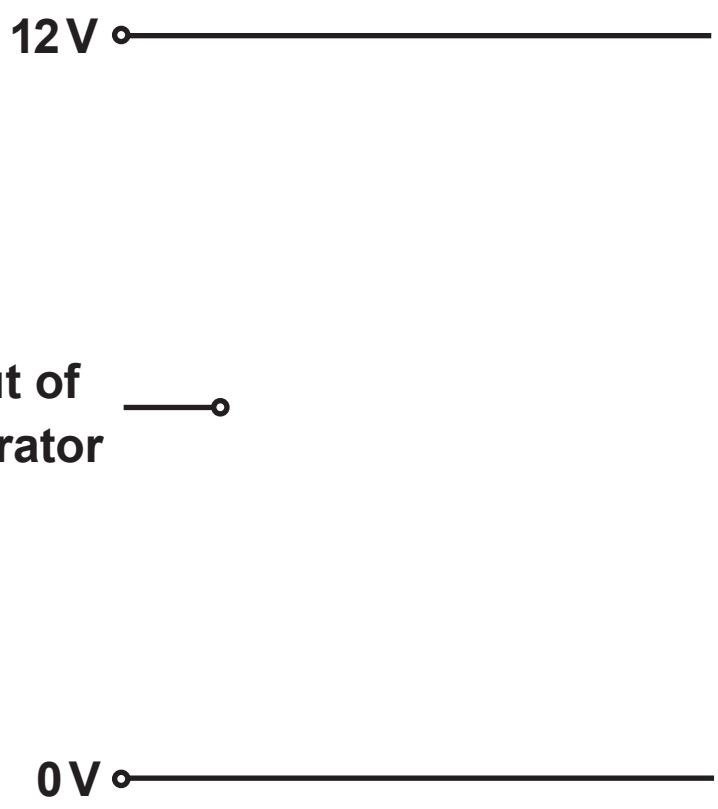


R_T = _____

V_T = _____

6(b) **The water is changed and is heated up from cold. With reference to V_T and V_X explain how V_{OUT} changes when the temperature increases from 20 °C to over 25 °C. [4]**

6(c) The student decides to use a MOSFET to operate the heater which is rated at 12 V, 48 W. Draw a suitable circuit below. [2]



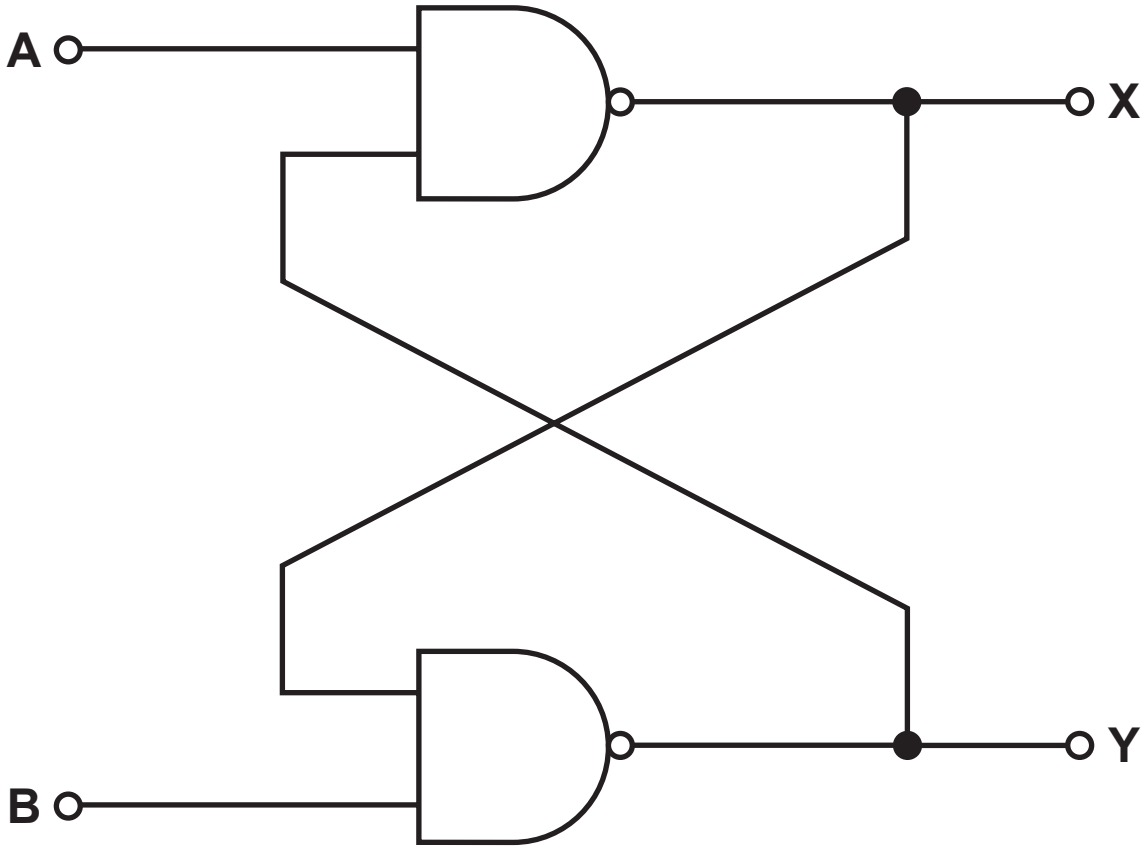
6(d) **The MOSFET has a maximum power dissipation of 60 W and r_{DSon} = 0.08 Ω.**

Calculate:

(i) **the minimum value of g_m to allow the heater to operate at its rated current. [3]**

6(d) (ii) **the power dissipated in the MOSFET when the heater is operating at its rated current.**

[2]

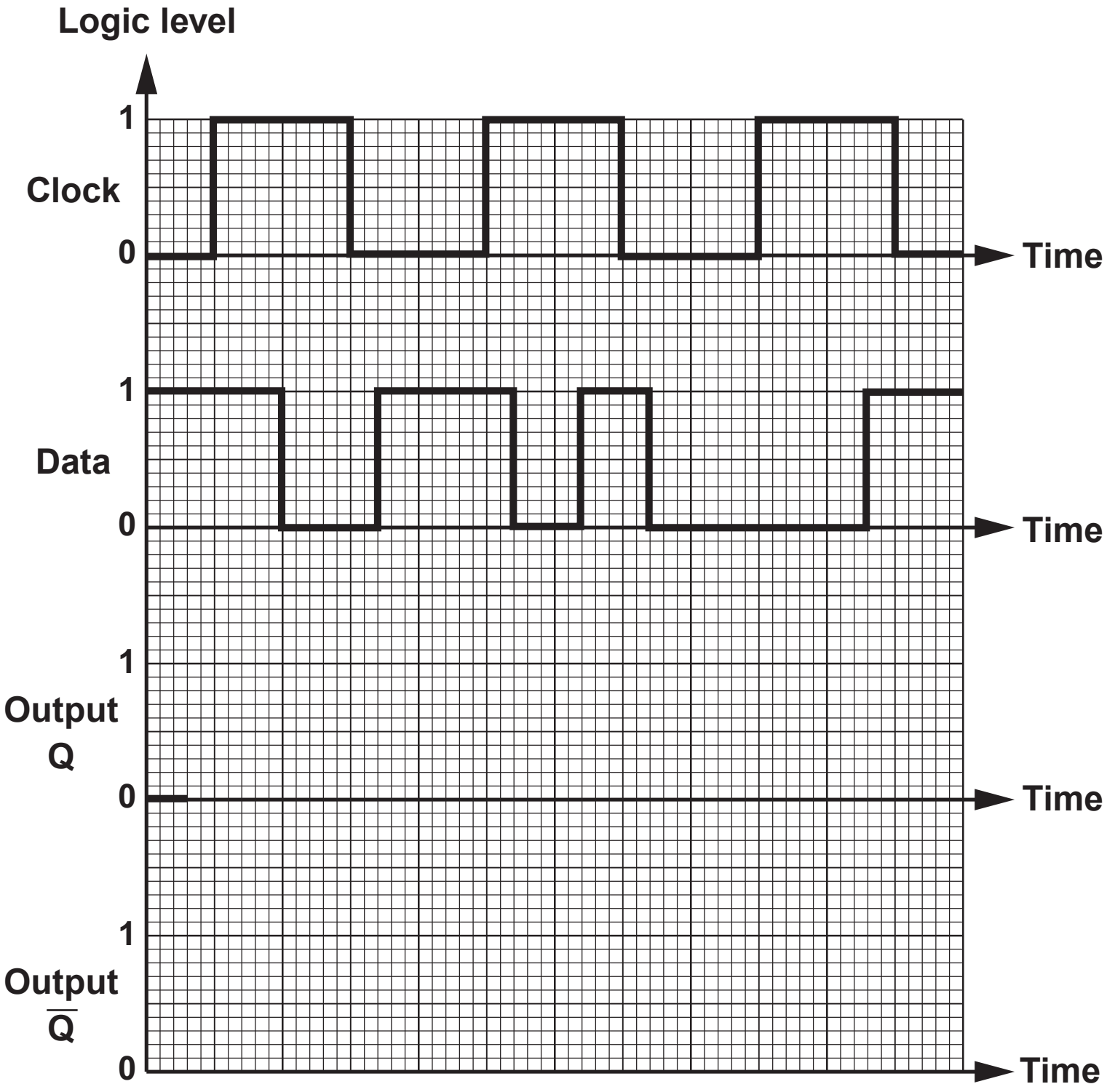

A
X
B
Y

7.(a) The following circuit shows a NAND gate bistable.

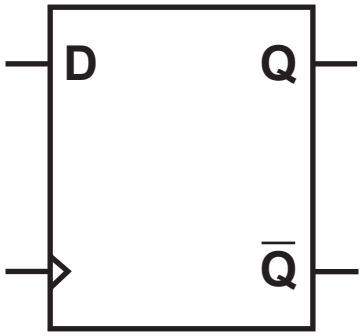
Complete the truth table to show the sequence of outputs at X and Y, for the given sequence of inputs A and B. [3]

A	B	X	Y
1	1	0	1
0	1		
1	1		
1	0		
1	1		
0	0		

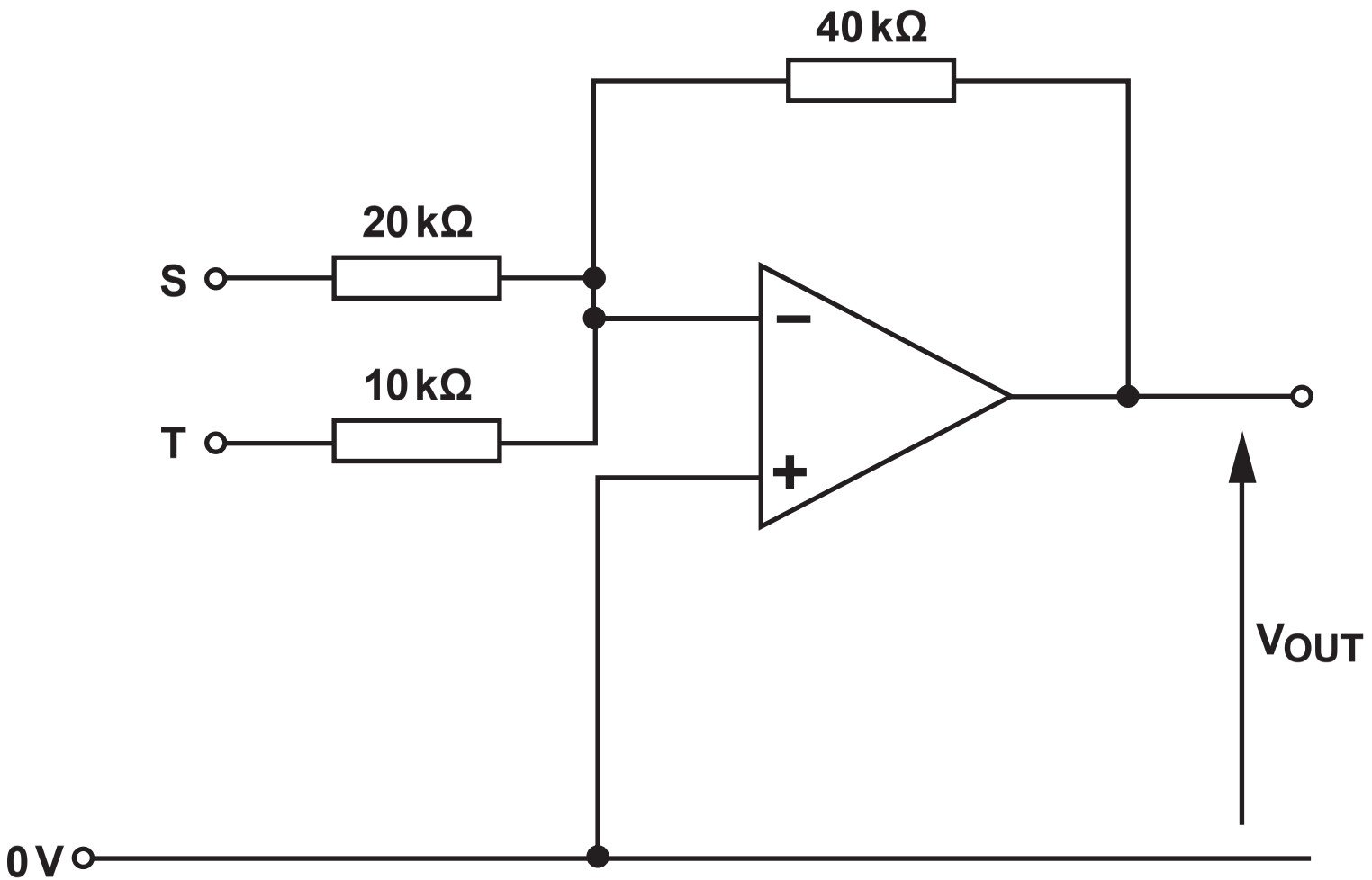
7(b) **The logic gates have a propagation delay of 10 ns. Explain what is meant by propagation delay. Then draw a transition gate in the space below constructed from NAND gates that produces the following pulse at its output when the input changes from logic 0 to logic 1. [4]**


Logic level
1
Clock
0
Time
1
Data
0
Time
1
Output
Q
0
Time
1
Output
$\overline{Q}$
0
Time

7(c) **The D-type shown in the diagram is rising-edge triggered.**



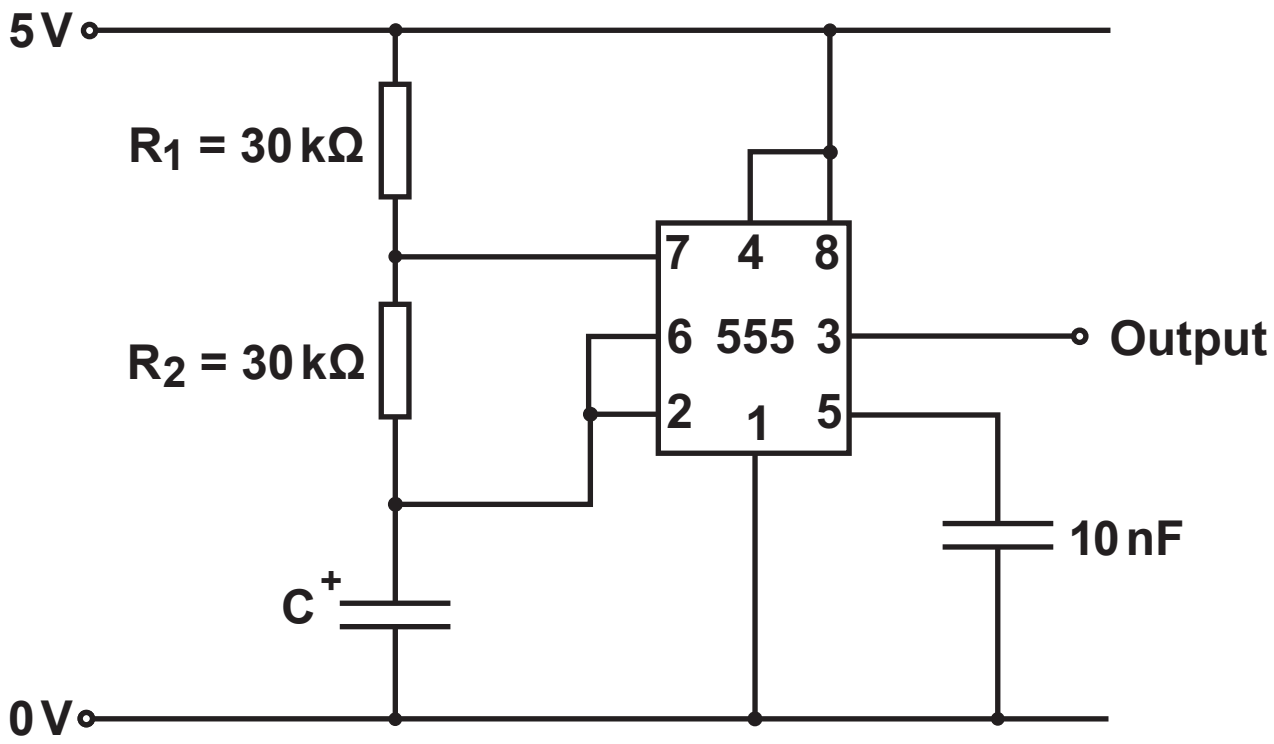
The signals applied to the clock and data inputs are shown opposite.
Complete the timing diagram for the Q and $\overline{Q}$ and outputs. **[3]**


40 kΩ
20 kΩ
S
10 kΩ
T
−
+
VOUT
0 V

8. **The circuit diagram opposite shows a summing amplifier. The output saturates at ±16 V.**

(a) **Calculate V_{OUT} when S = 2.0 V and T = 1.8 V. [2]**

(b) **Input S is kept at 2 V DC but input at T is replaced with the AC signal opposite.**
Draw the graph for V_{OUT}. [3]

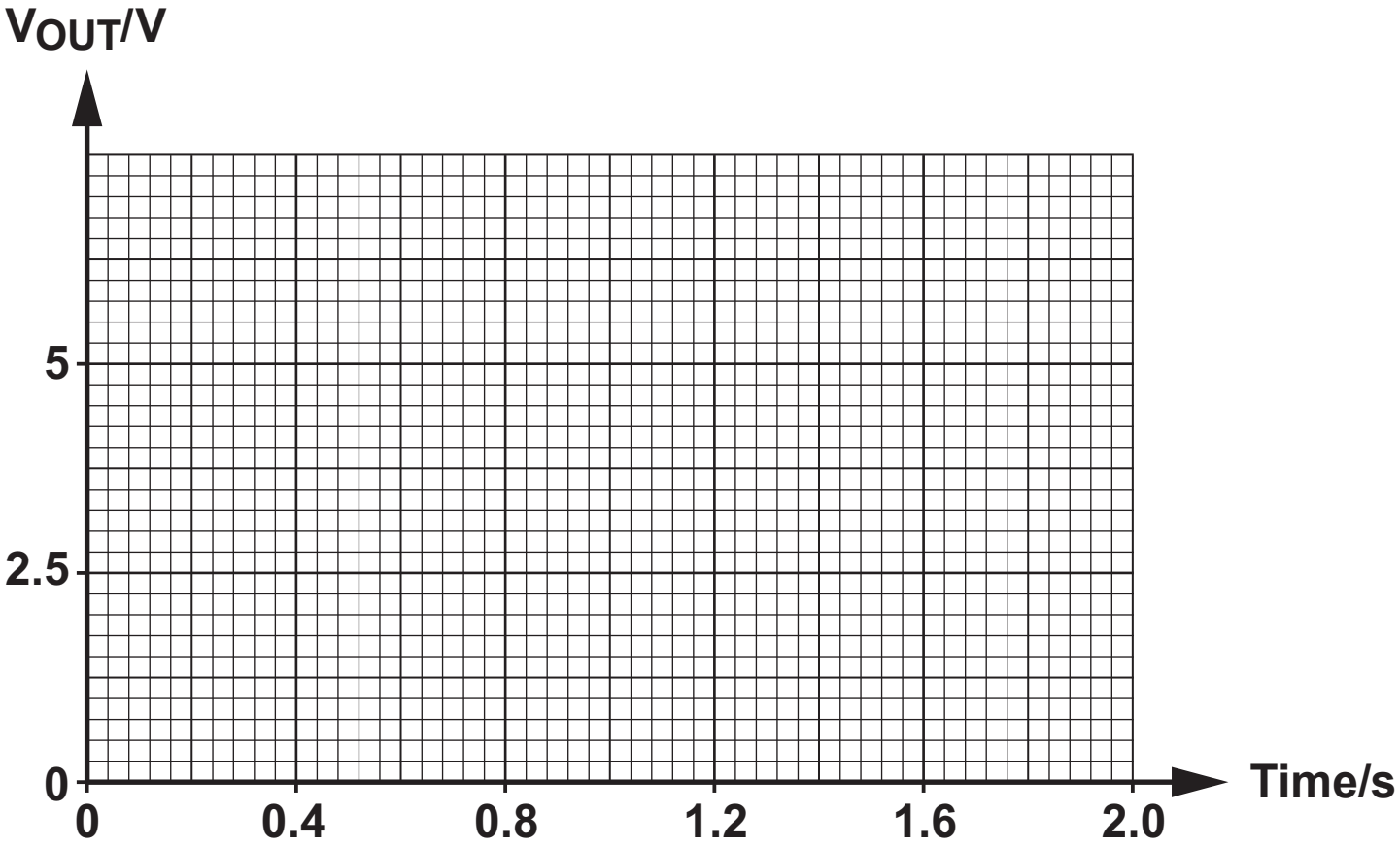

5 V
R1 = 30 kΩ
R2 = 30 kΩ
C
+
0 V
7
4
8
6
555
3
2
1
5
Output
10 nF

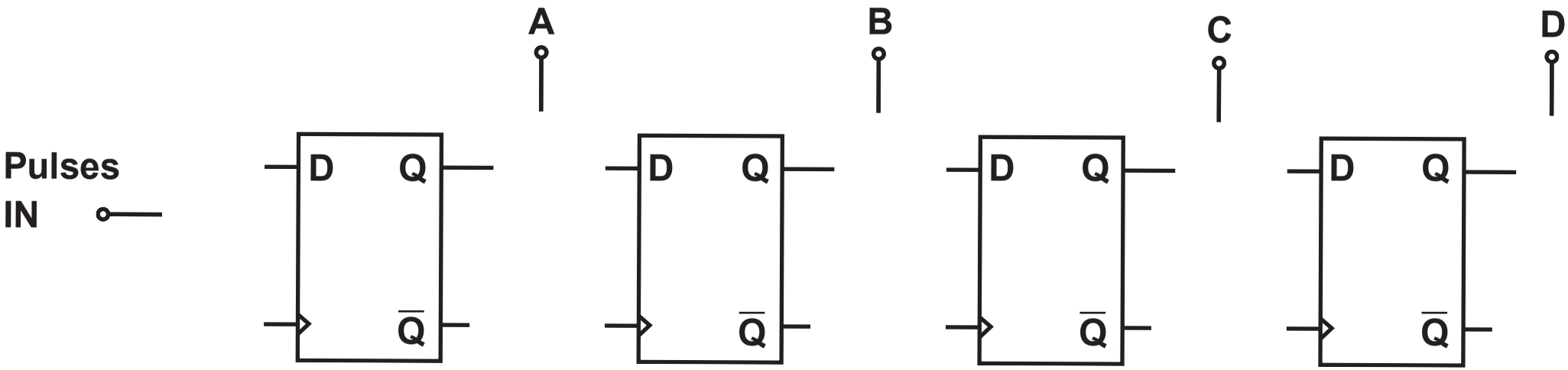
9. The following diagram opposite shows a 555 timer being used for an astable.

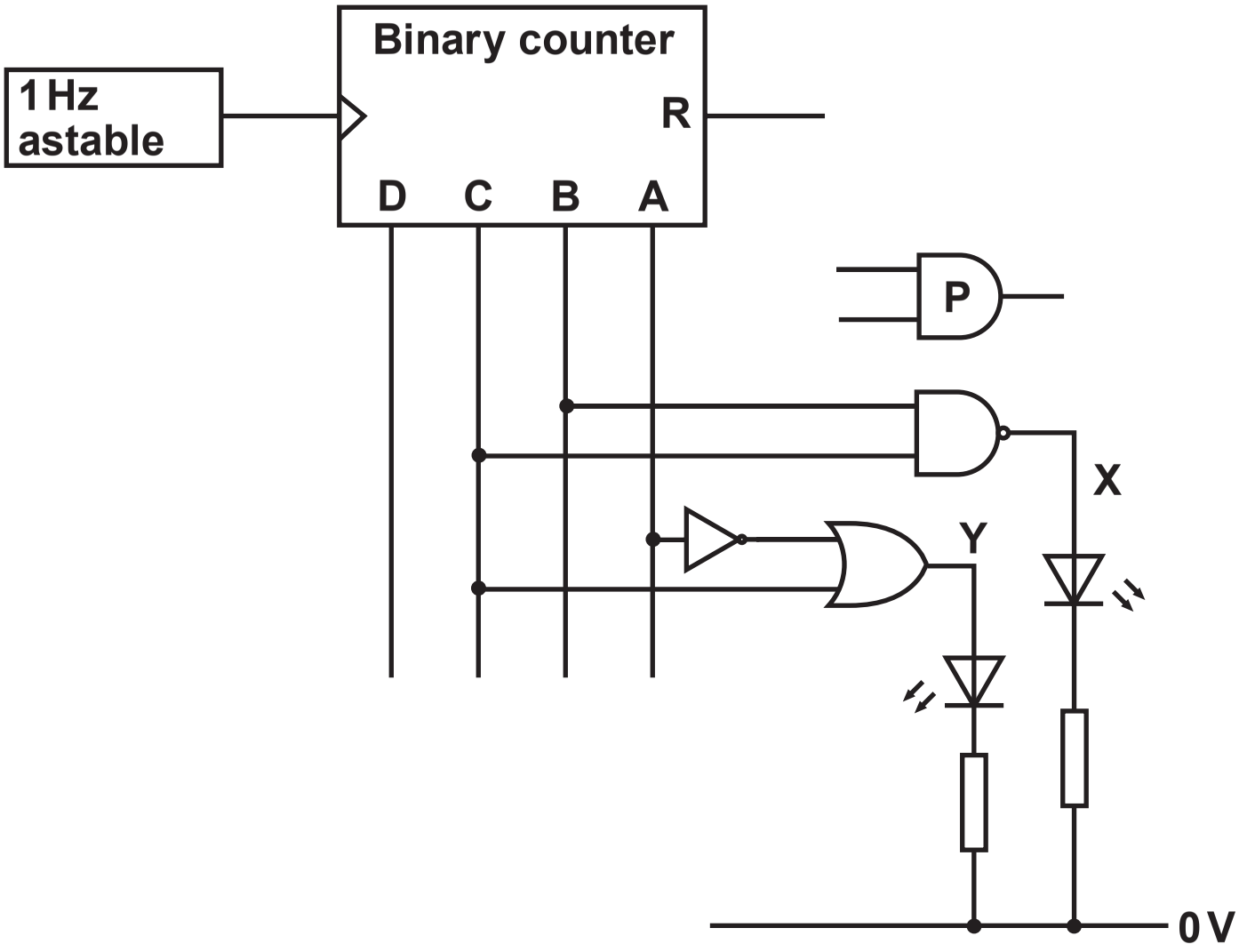
(a) (i) Calculate the value for capacitor C to produce an output signal with a frequency of 1 Hz. [3]

(ii) Calculate the mark/space ratio for this astable. [2]

9(a) (iii) **Use your answer to part (ii) to sketch TWO cycles of the output waveform from this astable. [2]**




Pulses
IN
A
B
C
D
D
Q
Q
D
Q
Q
D
Q
Q
D
Q
Q


1 Hz
astable
Binary counter
R
D
C
B
A
P
X
Y
0 V

9(b) **This diagram opposite shows RISING-EDGE triggered D-type flip-flops. Complete the diagram to make a 4-bit up-counter where A is the least significant bit. [3]**

(c) **A student designs a light sequencer using a dedicated binary counter with the 1 Hz astable feeding pulses into the counter.**

(i) **Complete the diagram opposite to make a counter that resets on the 9th pulse (modulo-9) using logic gate P. [2]**

(ii) **Complete the truth table opposite for the light sequencer. [3]**

Clock pulse	D	C	B	A	X	Y
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9						

9(c) (iii) **The system is reset. Describe what happens to LED X over a period of 8 seconds. [2]**


AC mains
S
C
R
VOUT

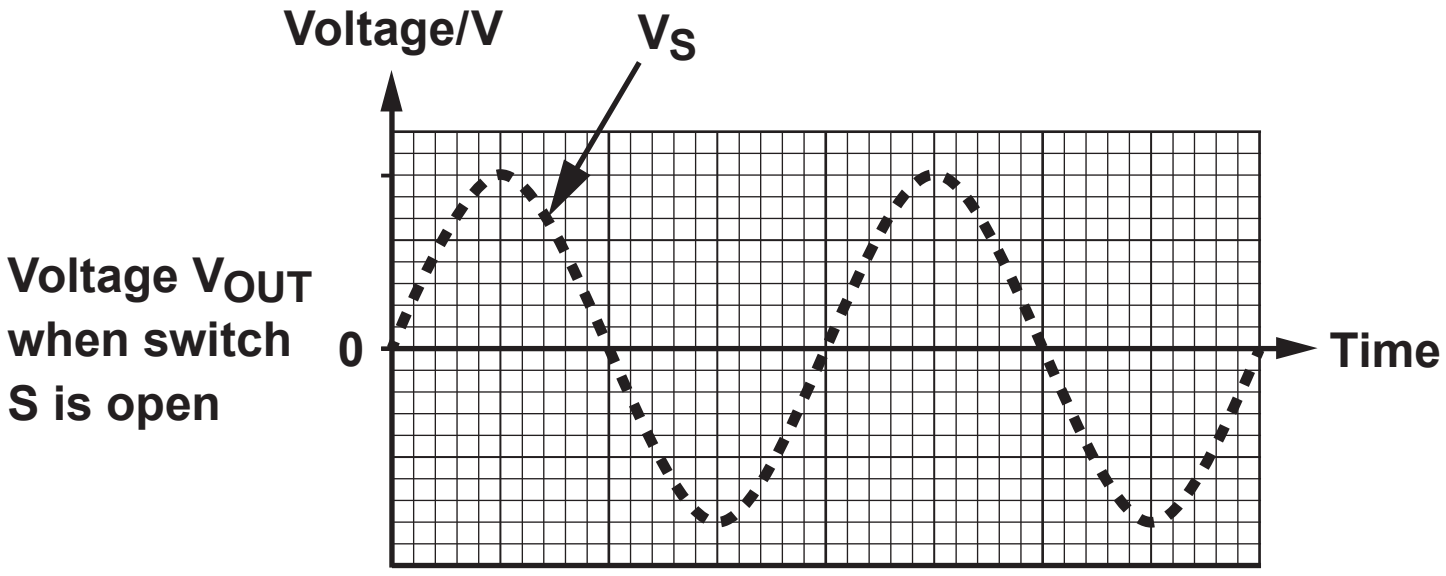
10. The diagram opposite shows an incomplete circuit for a full-wave rectified power supply.

(a) Add the components and connections necessary to complete the circuit. [3]

(b) The rms secondary voltage of the transformer is 8.5 V. Calculate the peak value of the secondary voltage and hence the peak value of the output voltage. [3]

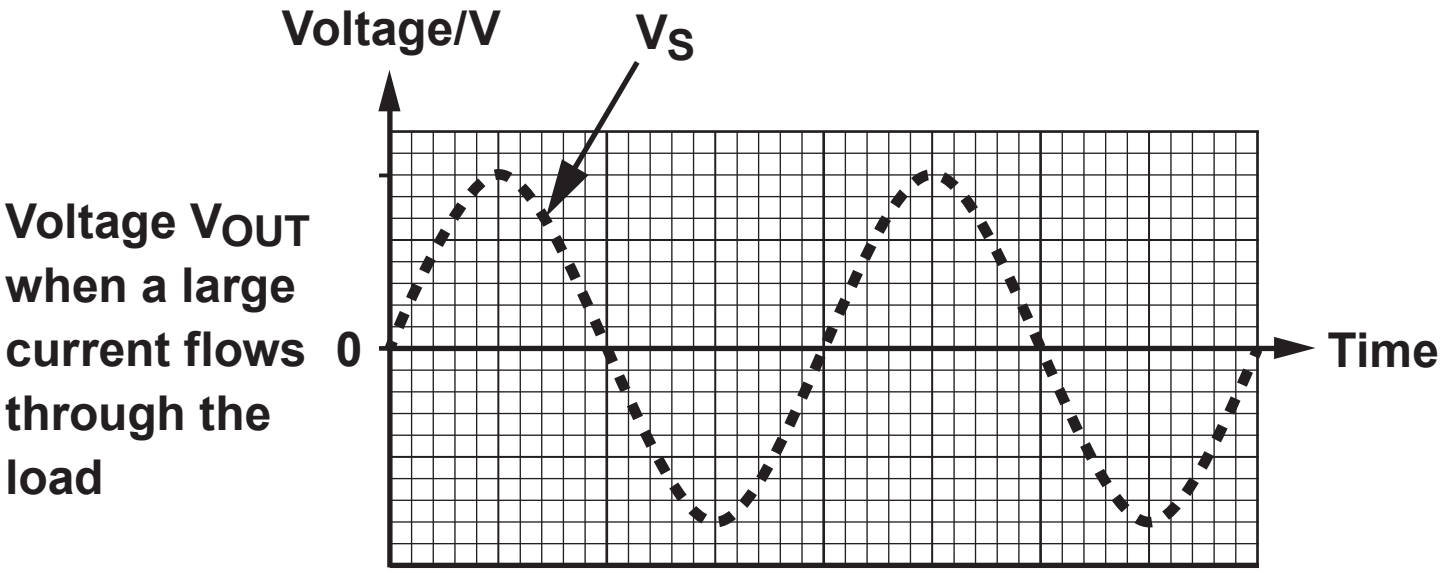
10(c) **On the axes provided below, sketch a graph to show the voltage V_{OUT} when switch S is open. Label the axes with any relevant voltages. [2]**

The voltage across the secondary windings of the transformer (V_S) is shown as a dotted waveform.

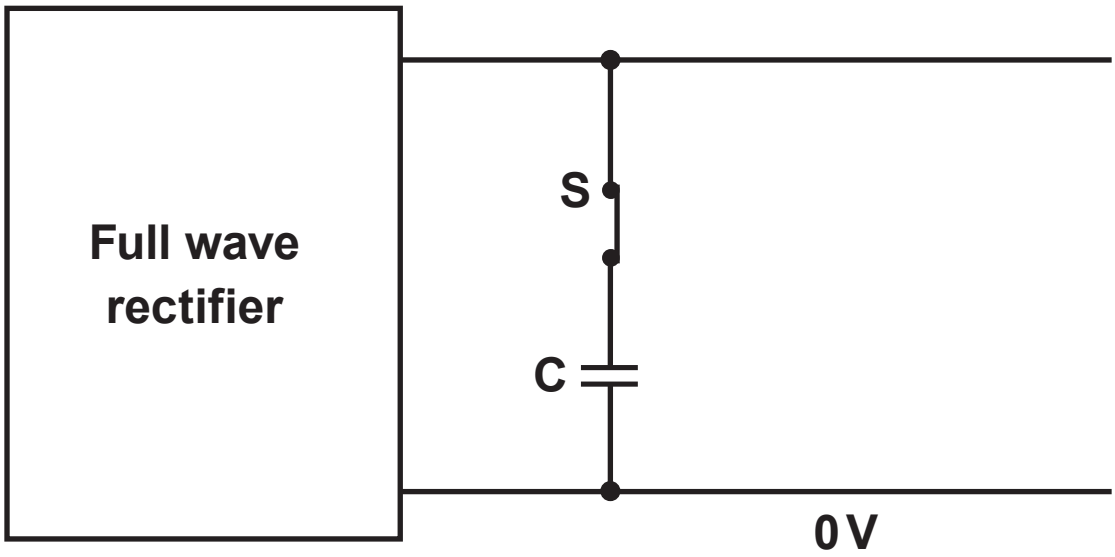


10(d) Switch S is now closed.

Use the next set of axes to sketch the voltage V_{OUT} when a large current flows through the load resistor, R. [2]



10(e) **The power supply is to be used to provide a regulated DC output. Draw a design for a Zener diode voltage regulator that can be added to the power supply to provide a steady 5.6 V output across a load resistor R.**
Complete the circuit clearly labelling all components added. No calculations are required.
[3]

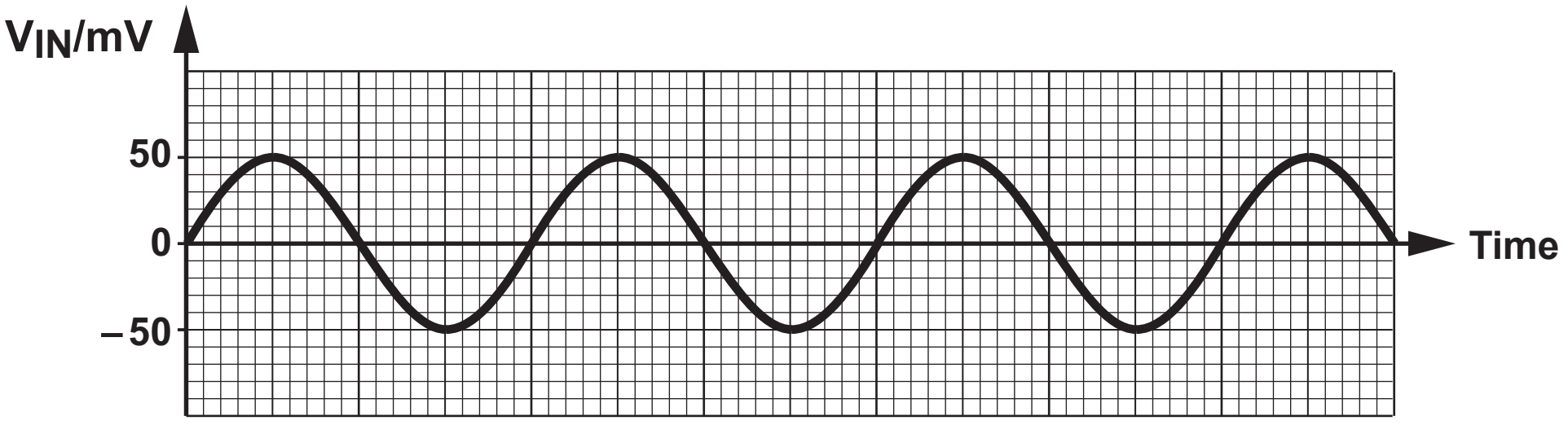


11. **An op-amp voltage amplifier is required that produces the output signal V_{OUT} shown in the graph opposite when signal V_{IN} is connected to its input.**

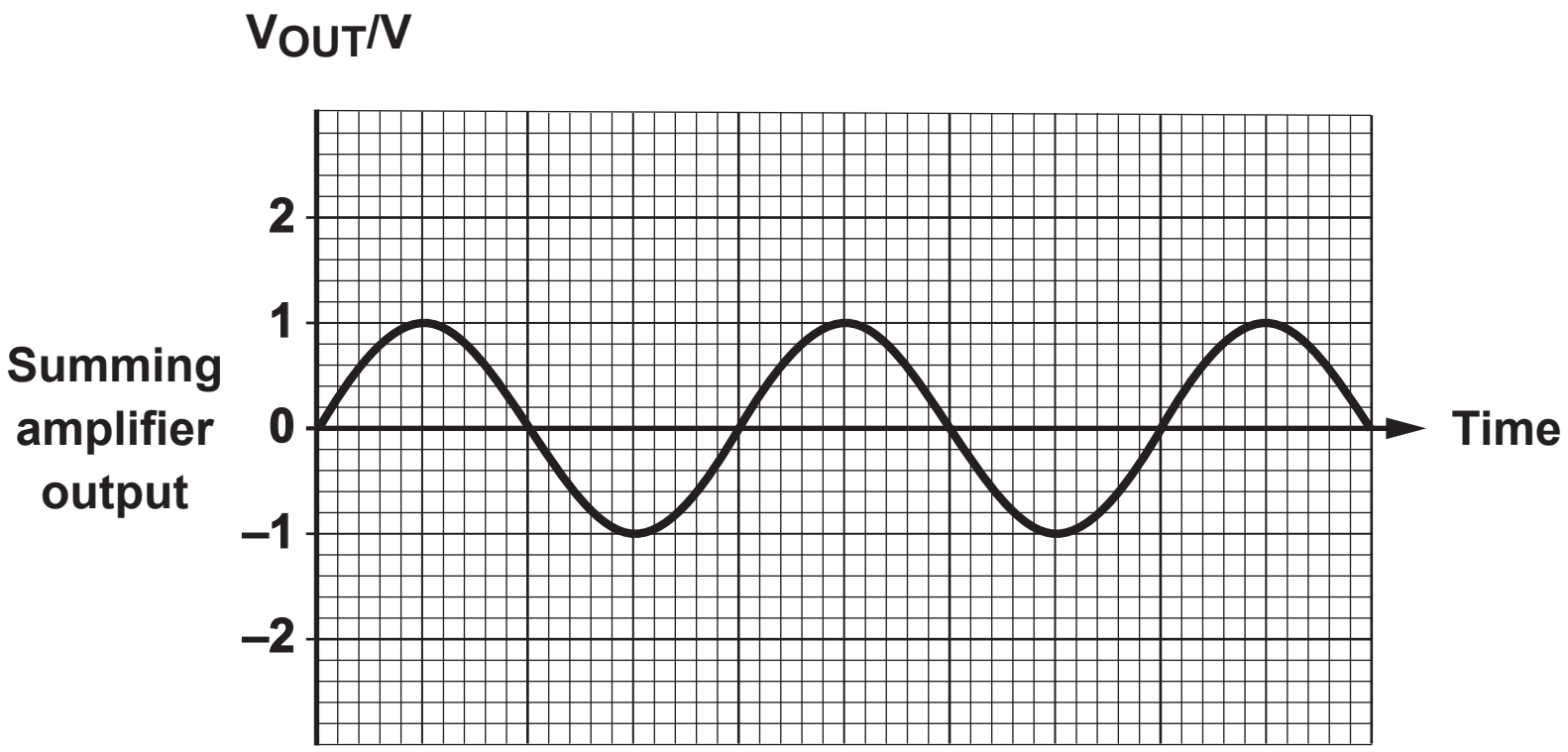
(a) **Use this op-amp to design an amplifier that will produce the output V_{OUT}. Your design should include a circuit diagram labelled with suitable resistor values. [6]**

11(b) Voltage amplifiers built from op-amps can produce signal distortion. Discuss how the limitations of op-amps and the circuits they are in gives rise to different types of distortion. Give details of the types of distortion, the effect that these have on the output voltage, and how such effects can be reduced or eliminated. [6 QER]

END OF PAPER


V_{IN}/mV
50
0
–50
Time

V_{OUT}/mV
1200
800
400
0
–400
–800
–1200
Time


V_{OUT}/V
2
1
0
–1
–2
Summing amplifier output
Time

V_T/V
20
15
10
5
0
–5
–10
–15
–20
Signal at T
Time