GCE A LEVEL – NEW

A490U20-1

MONDAY, 10 JUNE 2019 – AFTERNOON

ELECTRONICS – A level component 2

Application of Electronics

2 hours 45 minutes plus your additional time allowance

Surname _____

Other Names _____

Centre Number _____

Candidate Number 2 _____

For Examiner's use only		
Question	Maximum Mark	Mark Awarded
1.	13	
2.	17	
3.	20	
4.	14	
5.	19	
6.	16	
7.	11	
8.	14	
9.	16	
Total	140	

ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a DATA BOOKLET.

INSTRUCTIONS TO CANDIDATES

Use black ink, black ball-point pen or your usual method.

Answer ALL questions.

Write your name, centre number and candidate number in the spaces provided on the front cover.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in question 3(c).

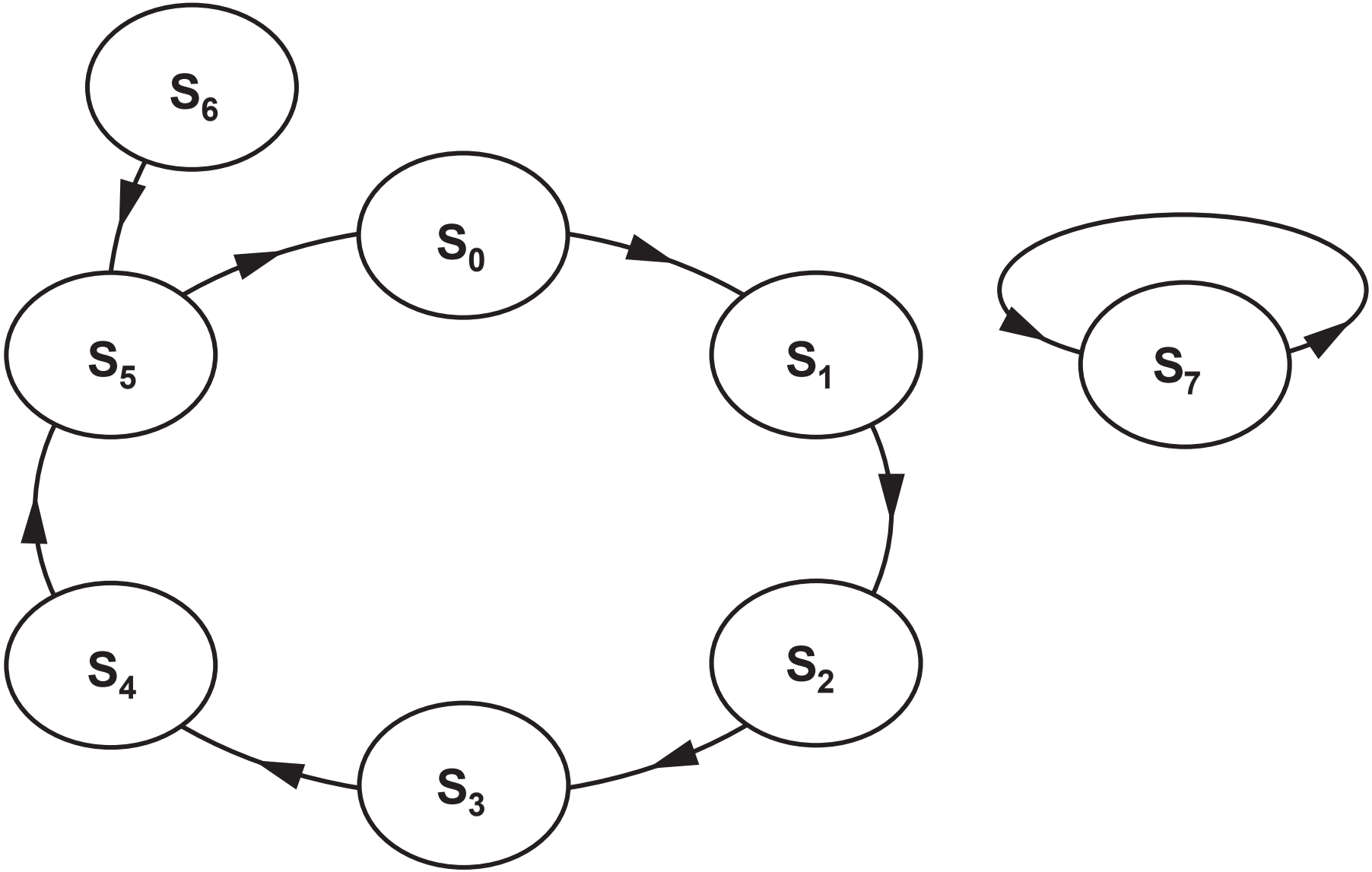
Answer ALL questions.

1(a) **The state diagram for a sequence generator is shown in the diagram opposite:**

(i) **The sequence is controlled by a 2 Hz clock.**

The sequence generator has been running for a while.

How long does it take to complete each cycle of the main sequence? [2]


S6
S0
S5
S1
S7
S4
S2
S3

1(a) (ii) States S_6 and S_7 are both unused.

Explain the difference between them. [2]

1(b) Part of the truth table for a DIFFERENT sequence generator is given opposite:

(i) Complete the table. [1]

(ii) Write down a Boolean expression for D_B in terms of C, B and A.

Then simplify it so that it uses only two gates. [2]

Raw expression: D_B = _____

C \ BA	00	01	11	10
0				
1				

State	Current Outputs			Next Outputs		
	C	B	A	D_C	D_B	D_A
0	1	0	1		1	
1	0	1	0		0	
2	1	0	0		1	
3	0	1	1		0	
4	0	0	0	1	0	1
5	0	0	1	1	0	1
6	1	1	0	1	0	0
7	1	1	1	1	0	0

1(c) **The circuit diagram for a THIRD sequence generator is shown opposite:**

(i) **Use this diagram to obtain Boolean expressions for D_C, D_B and D_A in terms of C, B and A. [3]**

D_C = _____

D_B = _____

D_A = _____

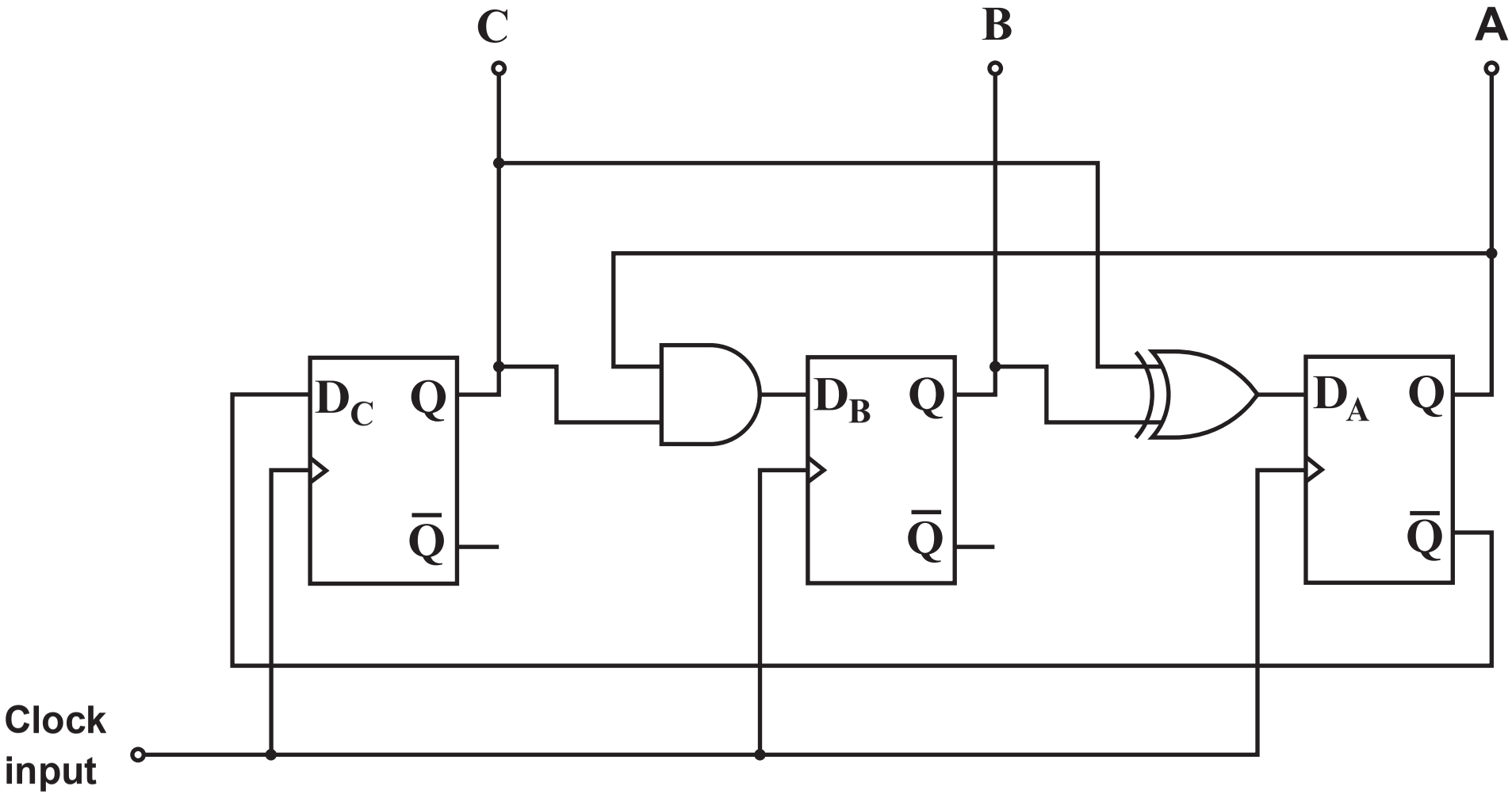
(ii) **On power up, the system starts in the state $C = 1$, $B = 0$, $A = 1$.**

The clock then inputs one pulse.
What state is the system now in? [3]

C = _____

B = _____

A = _____


C
B
A
D_C
Q
$\overline{Q}$
D_B
Q
$\overline{Q}$
D_A
Q
$\overline{Q}$
Clock
input

2.(a) The block diagram for a PIC microcontroller is shown opposite:

(i) Which block contains the whole program? [1]

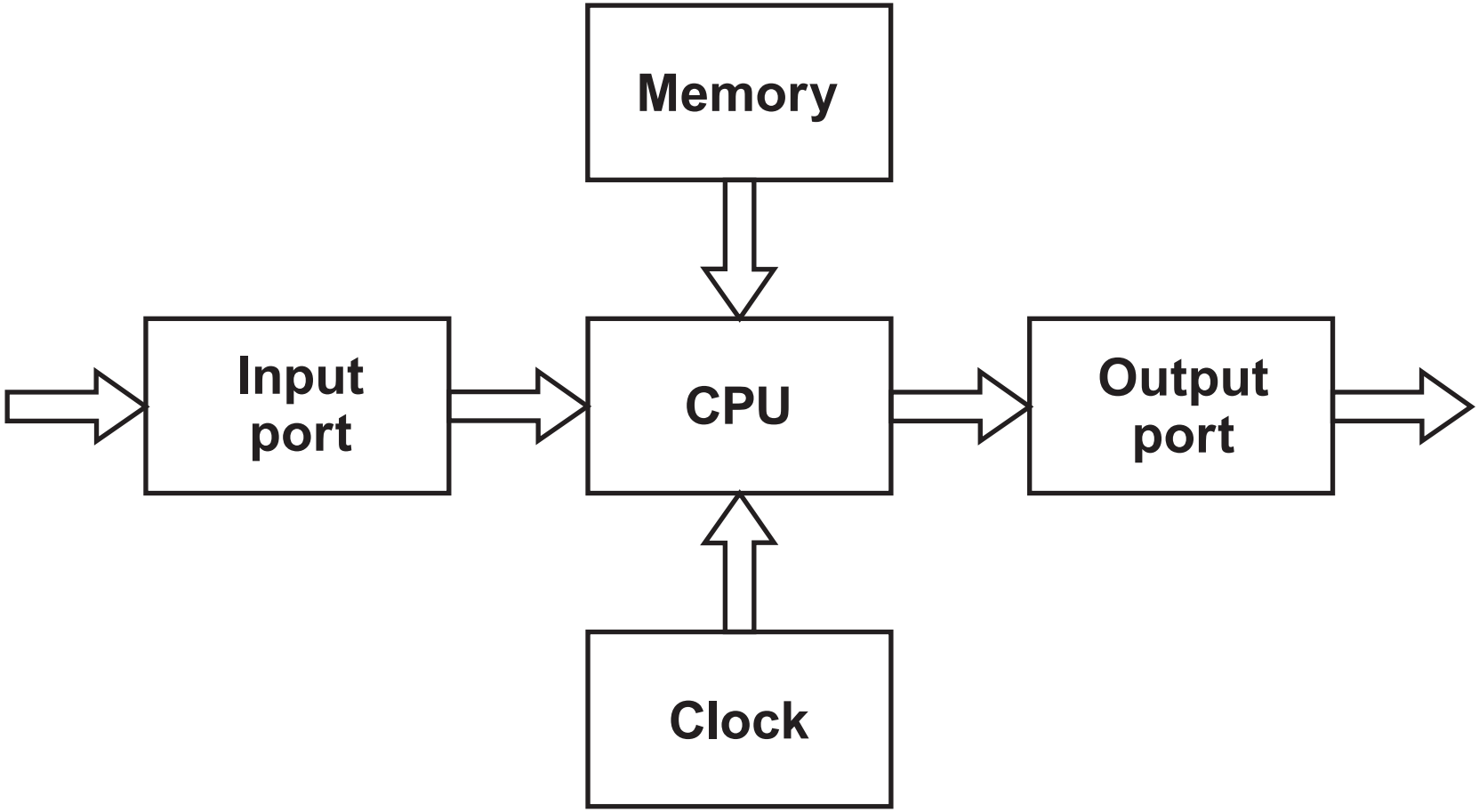
_____

_____

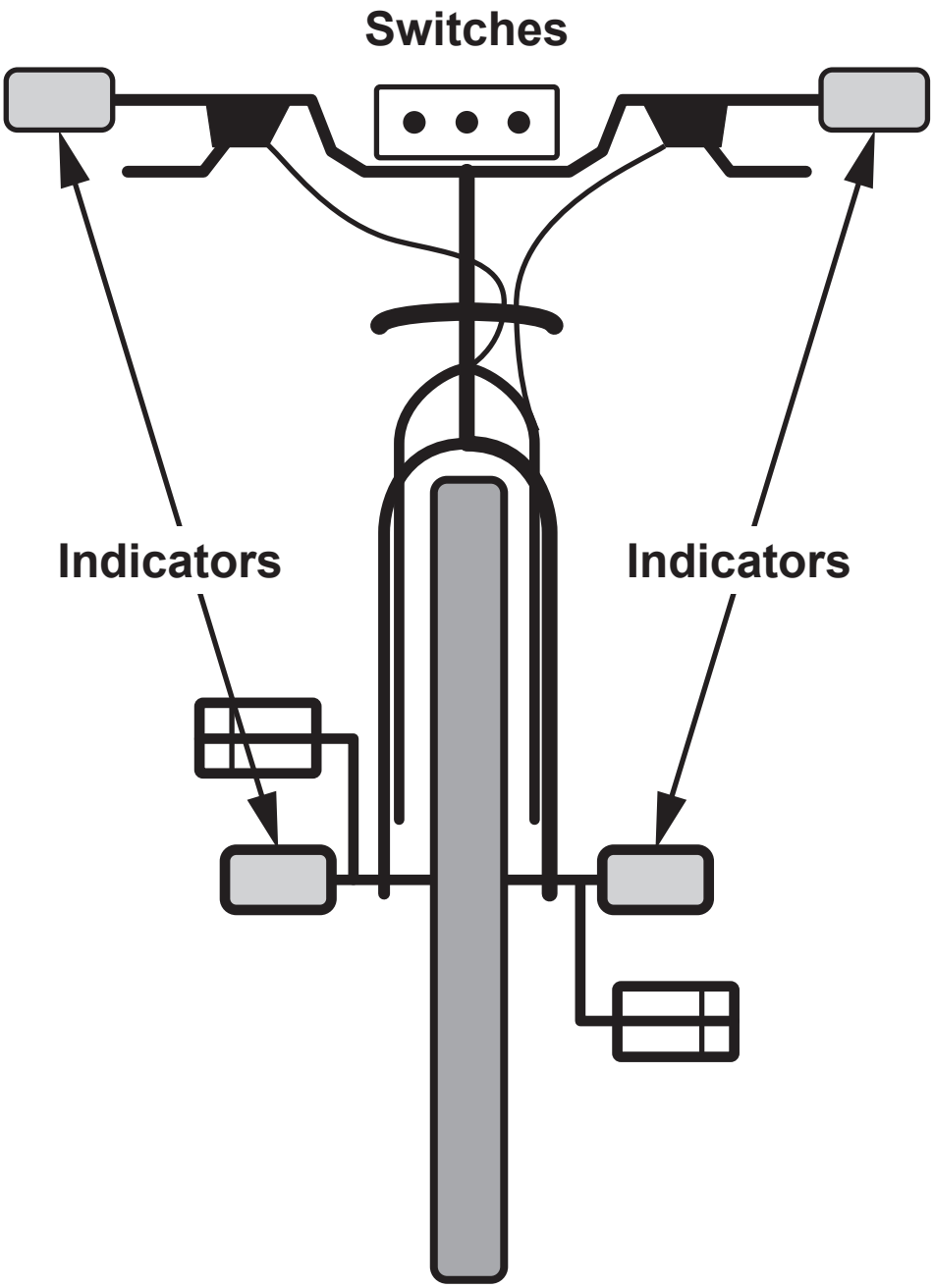
(ii) Which block has the task of synchronising data transfer and manipulation? [1]

_____

_____


Memory
Input port
CPU
Output port
Clock

2(b) **A student designs a direction indicator system for a bicycle.**



It has:

- **four LED lamps - two, at the ends of the handlebars, pointing forwards and two, either side of the rear wheel, pointing backwards;**

- **three switches, mounted at the centre of the handlebars;**

    - **one to operate the front and rear left-hand LED lamps, to indicate a left turn;**

    - **one to operate the front and rear right-hand lamps, to indicate a right turn;**

    - **one to turn on all LED lamps as a ‘hazard warning’.**

When a LED lamp is switched on, it flashes at a frequency of 2 Hz.

Pressing either ‘turn’ switch makes the corresponding LED lamp flash ten times and then stop.

Pressing the ‘hazard’ switch IMMEDIATELY flashes all four LED lamps.

2(b)(i) The ‘left-turn’ switch is connected to bit 0 of the input port, PORT A.

When the switch is pressed, it outputs a logic 1 signal.

The ‘right-turn switch’ is connected to bit 1 of PORT A.

Again, when pressed, the switch outputs a logic 1 signal.

The program checks whether the ‘left-turn’ or ‘right-turn’ switch has been pressed.

The subroutine ‘FLASH_LEFT’ causes the left-hand indicators to flash on and off ten times.

The subroutine ‘FLASH_RIGHT’ has the same effect on the right-hand indicators.

2(b) (i) Complete the code for that section: [5]

```
LOOP    btfsc    PORTA, _____
        call     FLASH_LEFT
        _____    _____
        call     _____
        goto     _____
```

```
FLASH_LEFT      movwf       WSTORE
                movlw       d’10’
REPEAT          movwf       COUNT
                movlw       d’5’
                movwf       PORTB
                call        QUART
                clrf        PORTB
                call        QUART
                decfsz      COUNT,F
                goto        REPEAT
                movf        WSTORE,W
                return
```

2(b) (ii) **The code opposite gives the subroutine which is called to operate the left-hand LED lamps. It uses a quarter-second delay subroutine called QUART.**

2(b)(ii) I. **Identify which port and which pins of that port are connected to the left-hand LED lamps. Explain how you arrive at your answer. [3]**

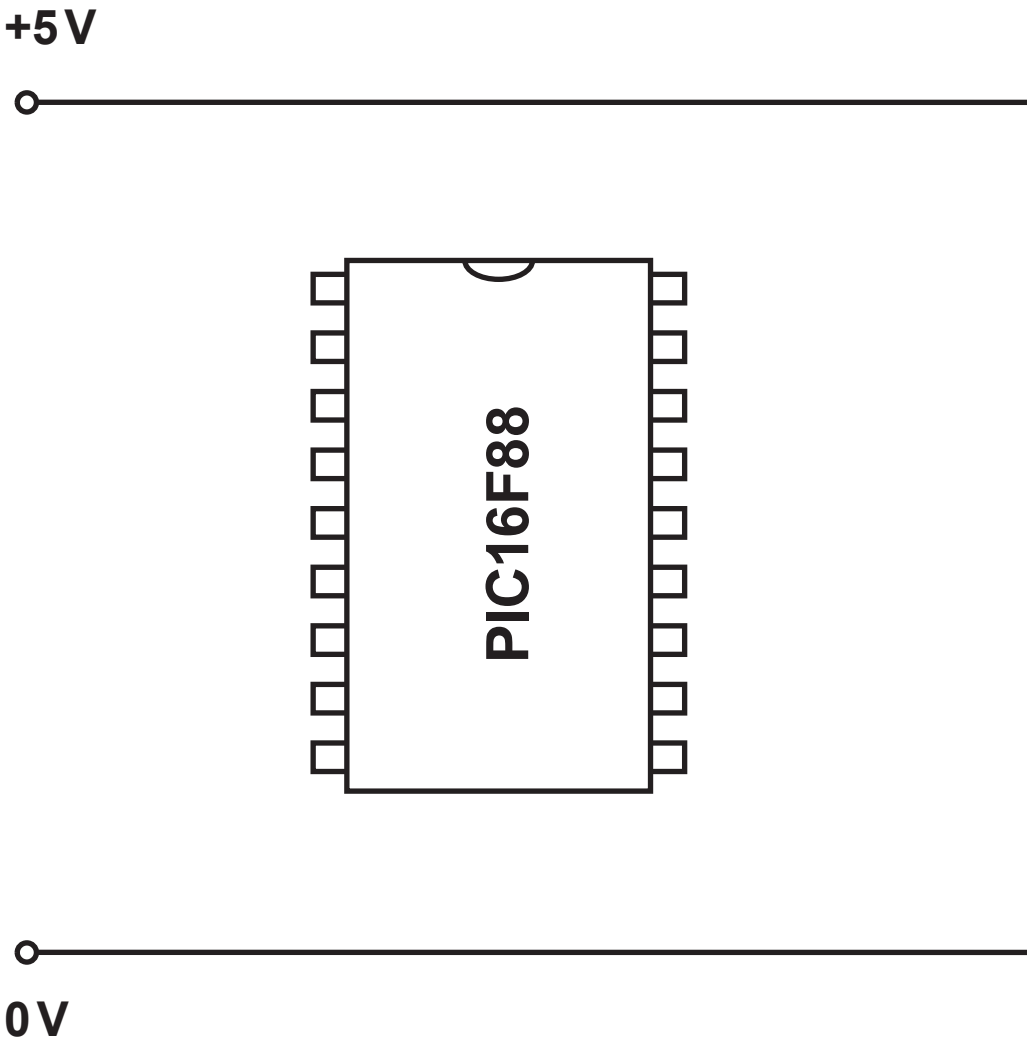
II. **Why are the instructions 'movwf WSTORE' and 'movf WSTORE,W' needed? [1]**

2(b)(ii) III. **What value is stored in the register 'COUNT' when the program completes the subroutine and returns to the main program? [1]**

2(c) (i) **The 'hazard' switch is connected to cause an interrupt when pressed.**

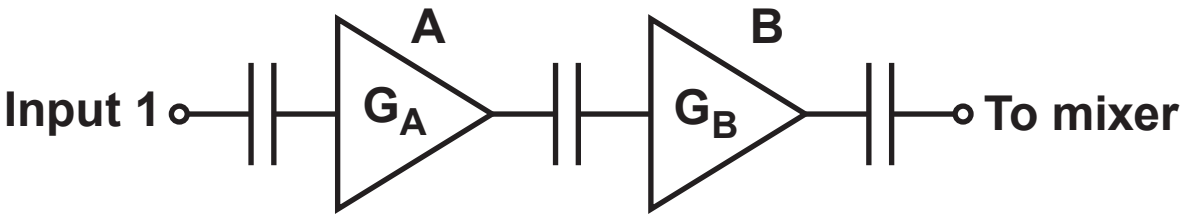
Why is it important that it is connected in this way, rather than it be polled during the main program? [2]

2(c) (ii) **Complete the circuit diagram opposite to show how the ‘hazard’ switch and any other component(s) needed are connected to the microprocessor. The switch is a ‘push-to-make’ type. [3]**

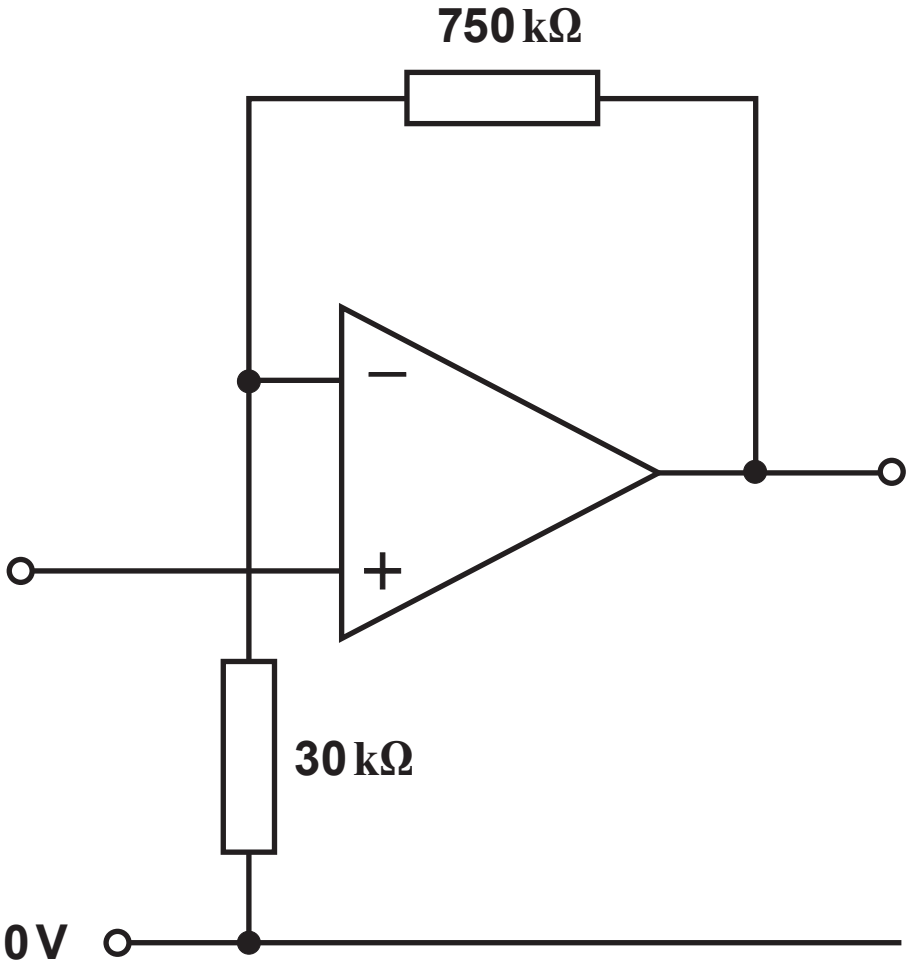

+5V
PIC16F88
0V

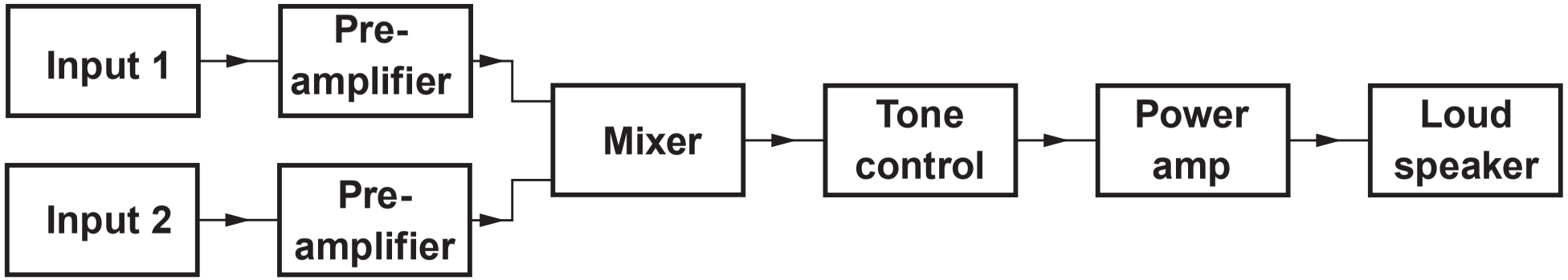
3. The diagram opposite shows the structure of an audio system.

(a) The preamplifier for INPUT 1 consists of two non-inverting amplifiers, as the diagram shows:



The circuit diagram for each is given below:




Input 1
Pre-
amplifier
Input 2
Pre-
amplifier
Mixer
Tone
control
Power
amp
Loud
speaker

3(a) (i) **The op-amps used have a gain-bandwidth product of 3 MHz.**

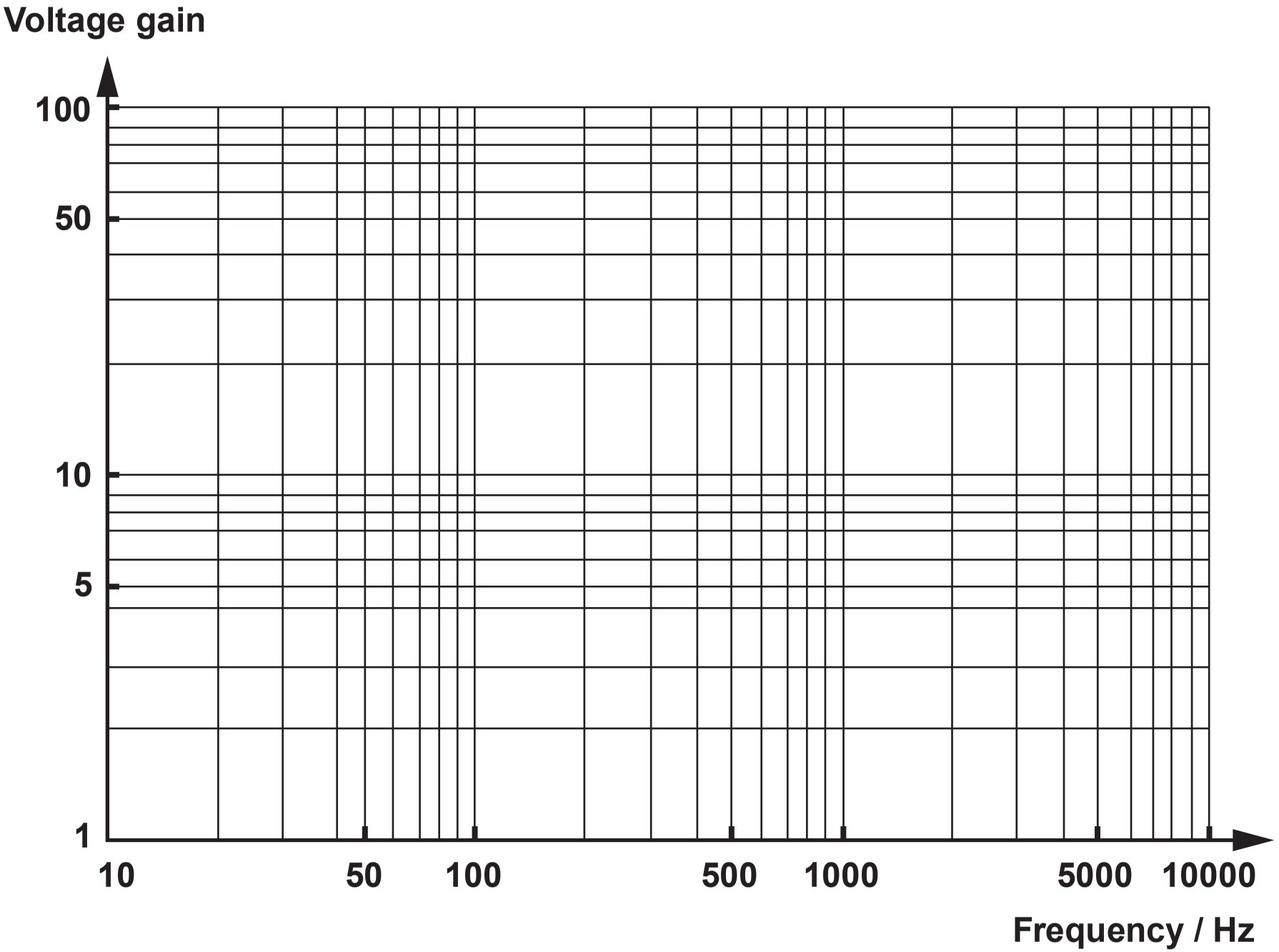
What is the overall voltage gain and bandwidth of the preamplifier? [5]

3(a) (ii) **The preamplifier includes three capacitors. What is their function in this circuit? [1]**

3(b) **A first order active filter is used in the tone control block to boost those parts of the signal with frequencies below 200 Hz.**

The filter gives all frequencies above this limit a voltage gain of 2.

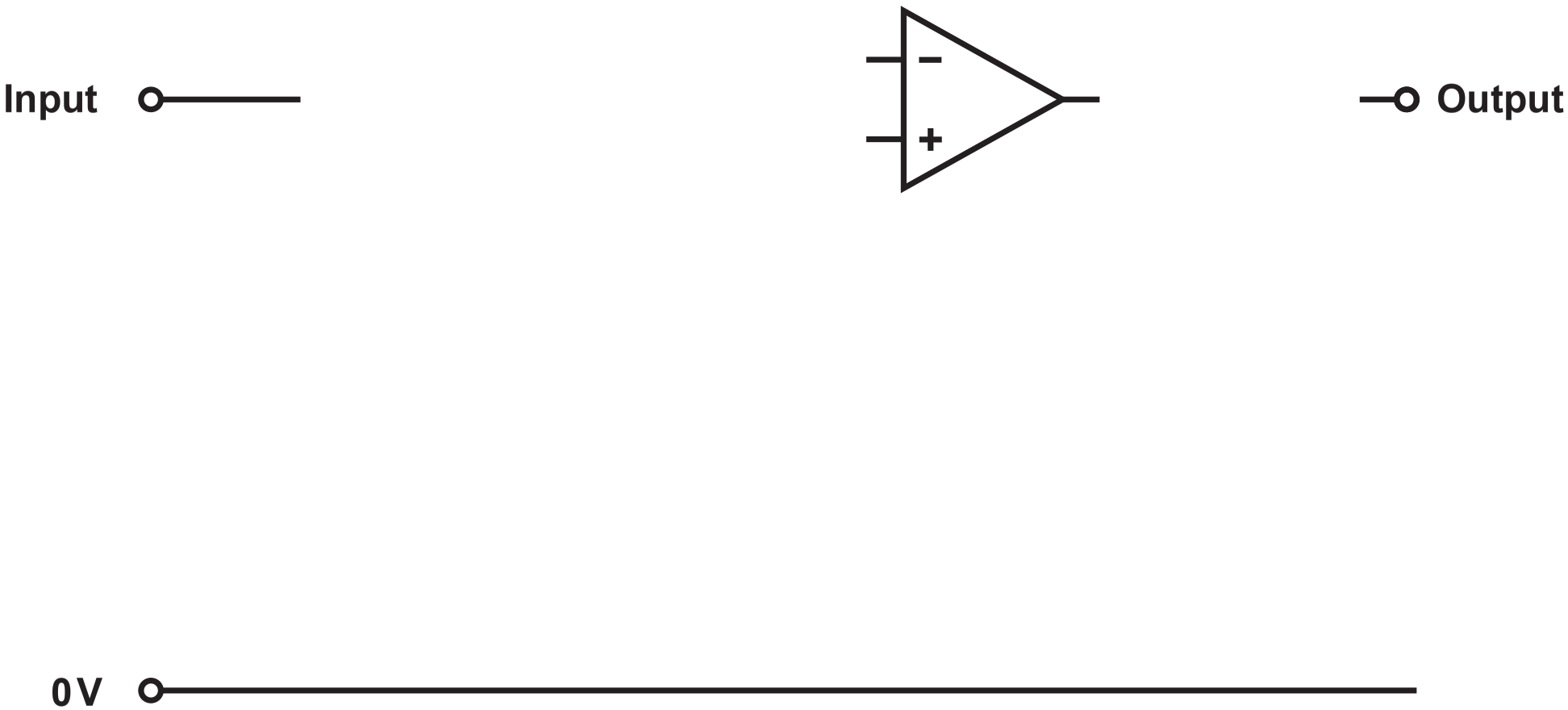
(i) **Use this information and the axes provided opposite to sketch the frequency response of this filter. [3]**


Voltage gain
100
50
10
5
1
10
50
100
500
1000
5000
10000
Frequency / Hz

3(b) (ii) **Design a suitable circuit for this filter to create the best possible fit to the specification, using the following components (and no others):**

- **an op-amp;**
- **a 39 kΩ resistor;**
- **a 82 kΩ resistor;**
- **a 10 nF capacitor.**

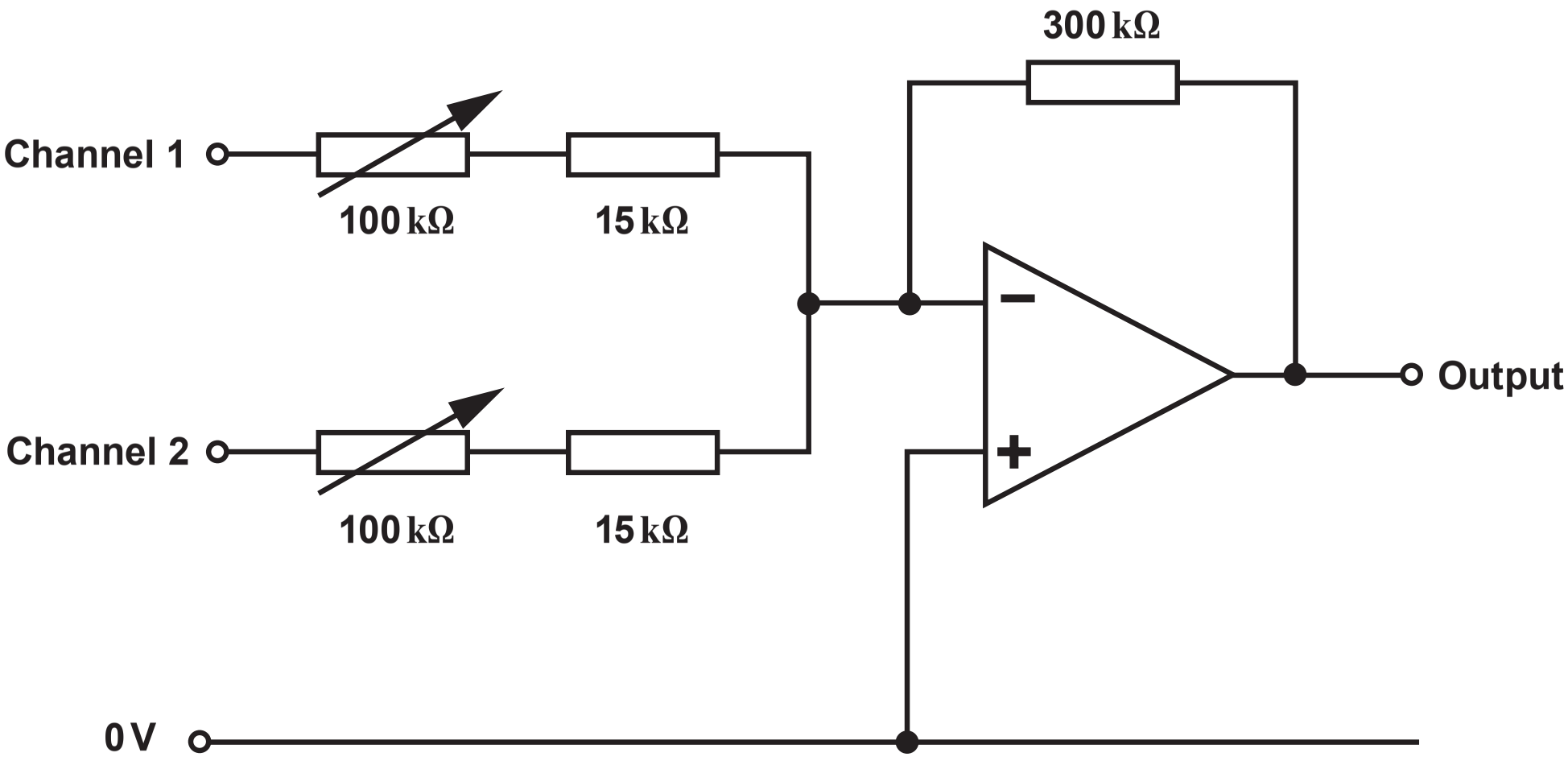
On the opposite page complete the circuit diagram for your design. [5]


Input
−
+
Output
0 V

3(c) Here is the specification for the audio system mixer:

Number of channels	**2**
Input impedance (both channels)	**>10 kΩ**
Voltage gain (both channels)	**variable from 2× to 20×**

The circuit opposite is proposed as a suitable solution.


300 kΩ
Channel 1
100 kΩ
15 kΩ
Channel 2
100 kΩ
15 kΩ
Output
0 V

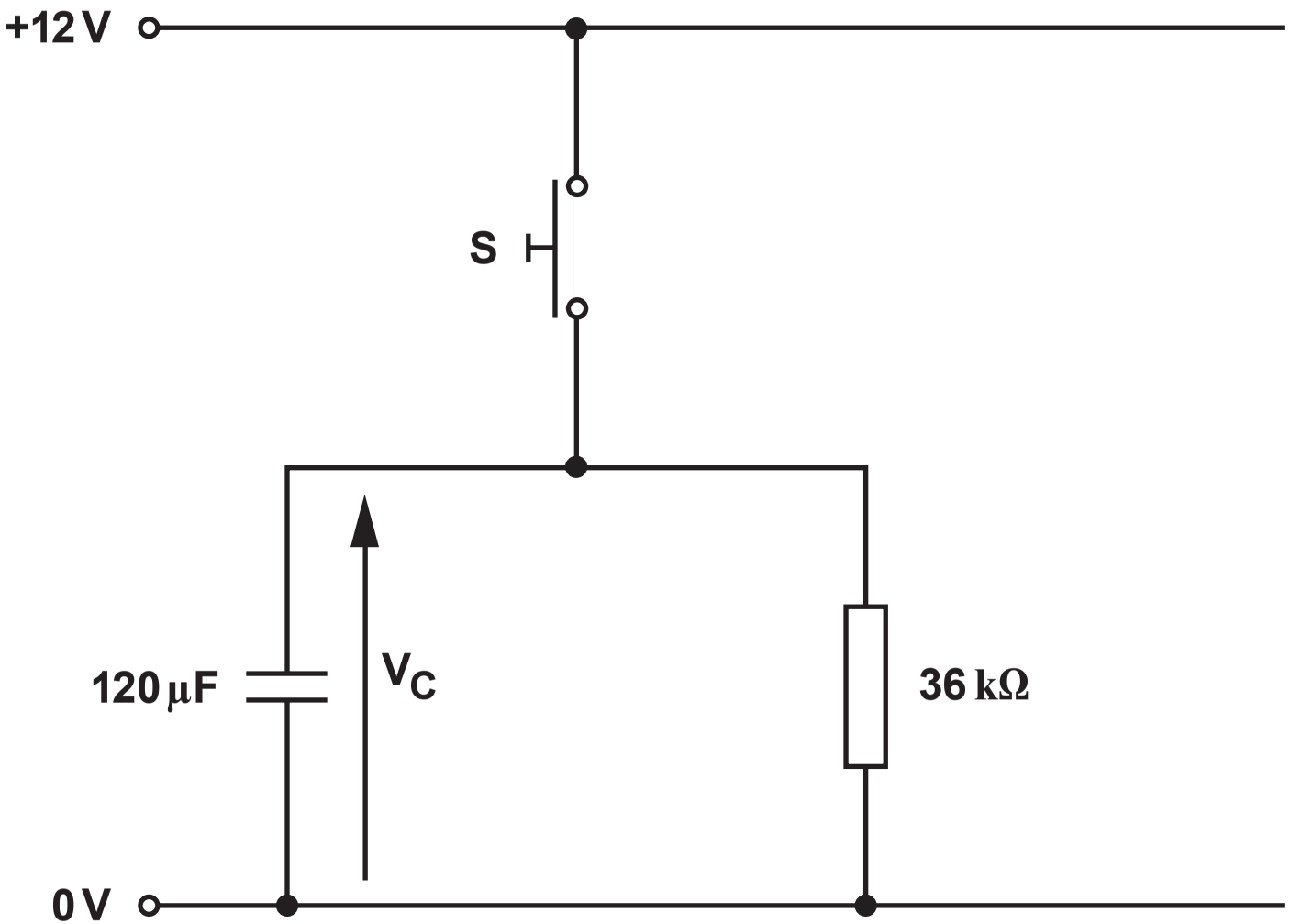
3(c) Evaluate this circuit as a solution that meets the specification given on page 21. [6 QER]

4. **A shop owner wants a buzzer to sound every time someone opens the shop door.**

One way to achieve this is to drive the buzzer from a NOT gate which is triggered by an input sub-system consisting of a RC network and a switch S, attached to the shop door frame (shown on opposite page).

(a) **The RC network uses a 120 μF capacitor and a 36 kΩ resistor.**

When the switch contacts close, the capacitor charges up immediately to +12 V.


+12 V
S
120 µF
V_C
36 kΩ
0 V

4(a) (i) Calculate the time constant of the RC network. [2]

(ii) Switch S is momentarily closed and then opened at time t = 0.

Determine the time taken for V_C to reach 6.0 V. [2]

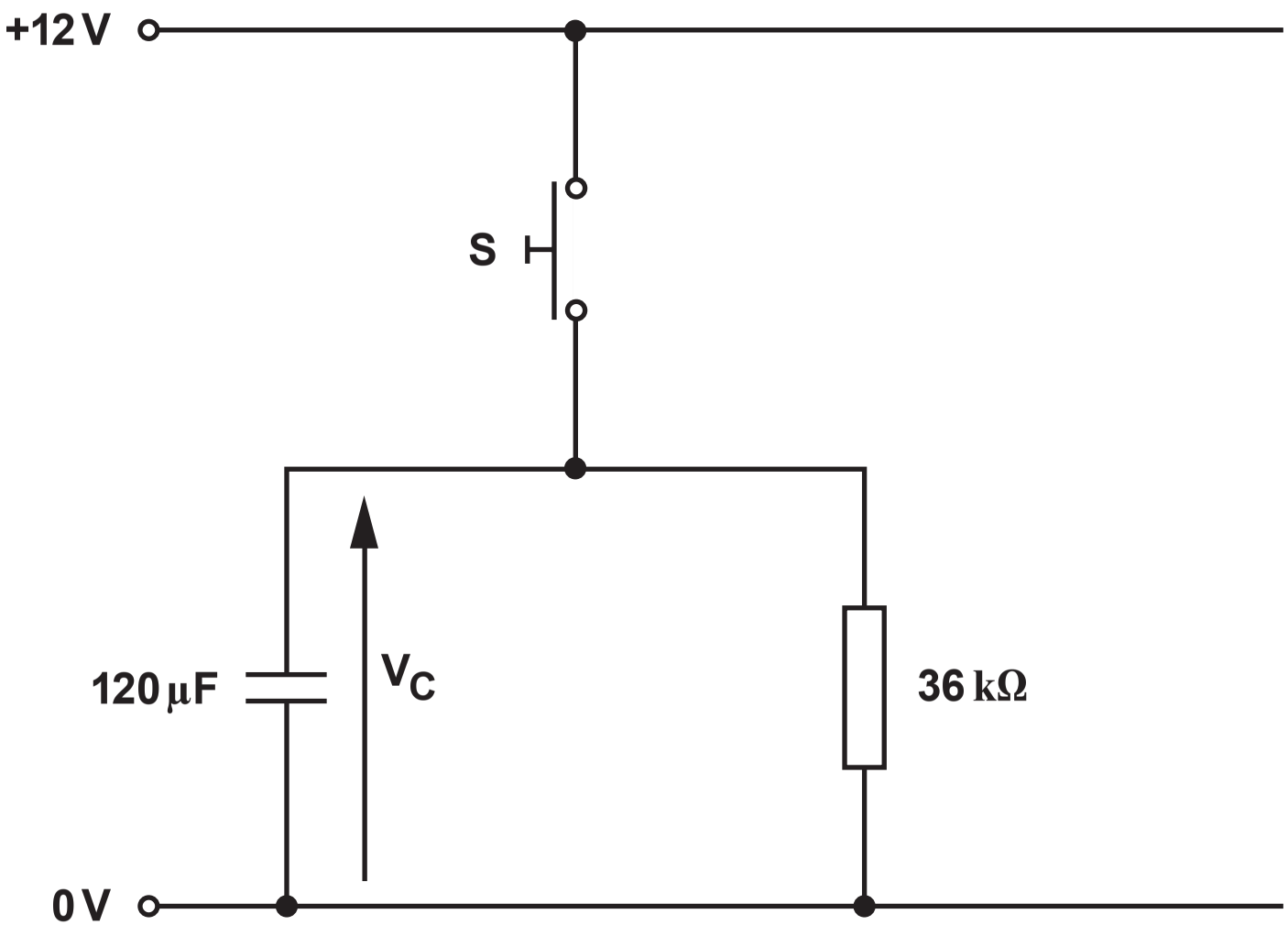
4(b) **When the shop door is closed, the switch contacts are OPEN. When the door opens, the contacts CLOSE.**

The NOT gate has a switching threshold of 6 V.

(i) **Complete the circuit diagram opposite by adding the NOT gate and buzzer. [2]**

(ii) **The shop door opens for five seconds, and then closes.**

For how long does the buzzer sound? Explain your answer. [2]


+12 V
S
120 µF
V_C
36 kΩ
0 V

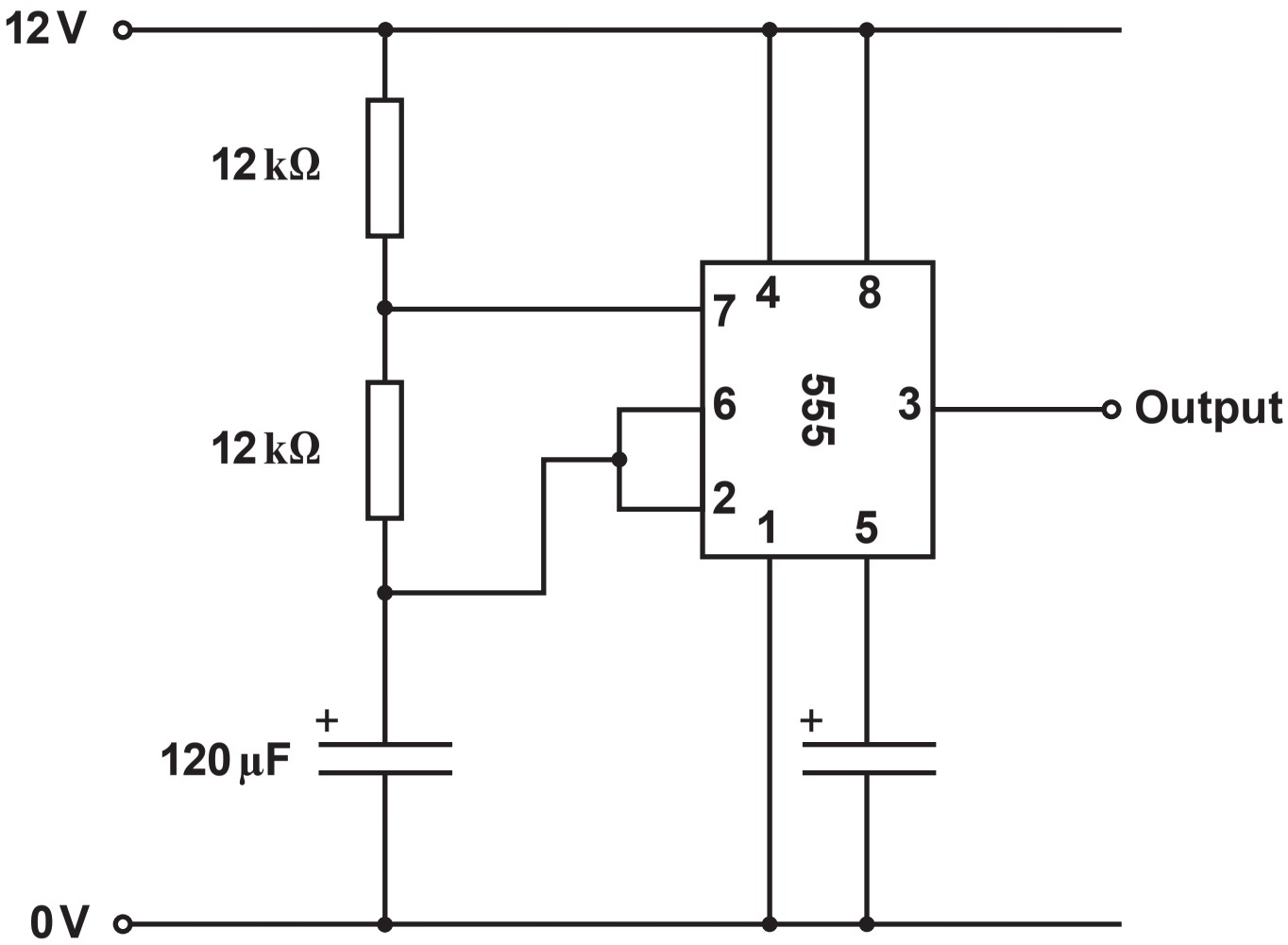
4(c) **After using the system for a while, the shop owner decides it would be more desirable to pulse the buzzer, rather than have it sound continuously.**

The circuit is modified accordingly, using the astable circuit shown opposite.

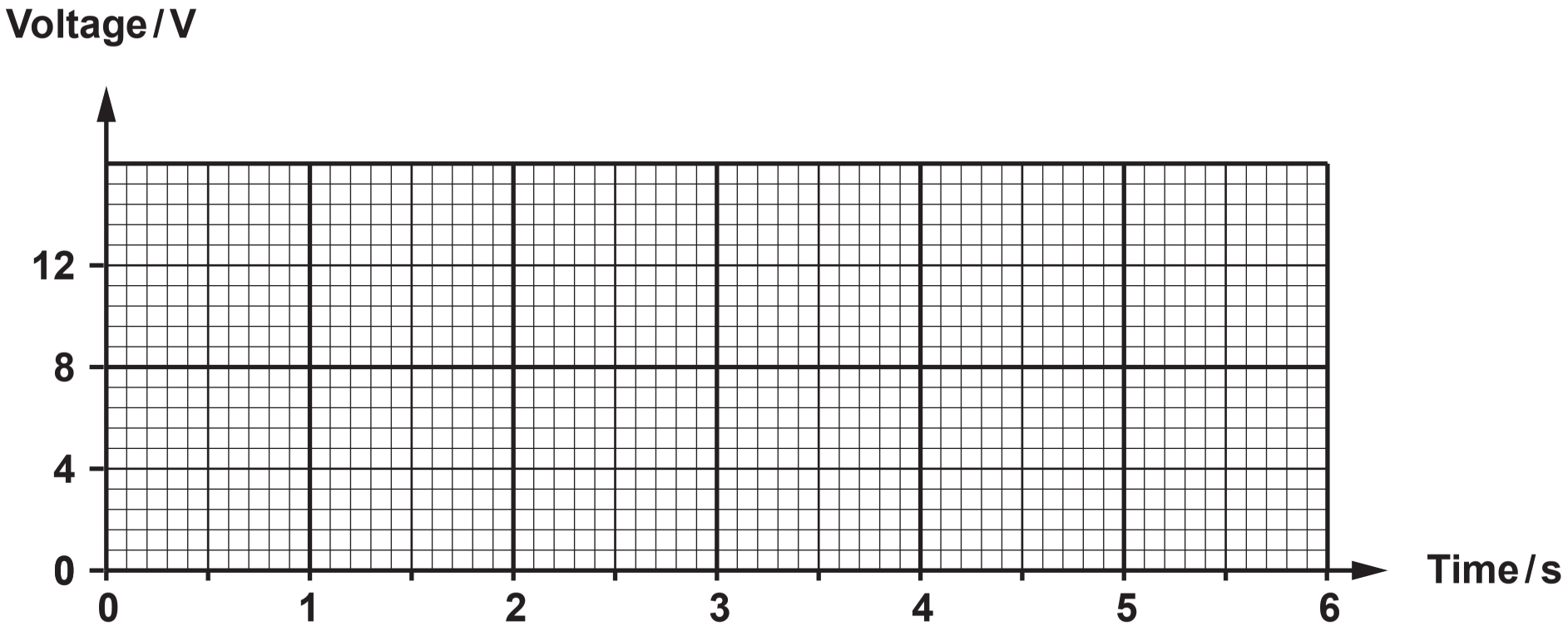
(i) **Calculate the frequency and mark:space ratio of this astable . [4]**

Frequency = _____Hz

Mark:space ratio _____


12 V
12 kΩ
12 kΩ
120 µF
0 V
555
Output
1
2
3
4
5
6
7
8

4(c) (ii) **Using the axes provided opposite, sketch a graph to show TWO cycles of the output signal produced by this astable, given that it pulses between 12 V and 0 V. [2]**


Voltage / V
12
8
4
0
0
1
2
3
4
5
6
Time / s

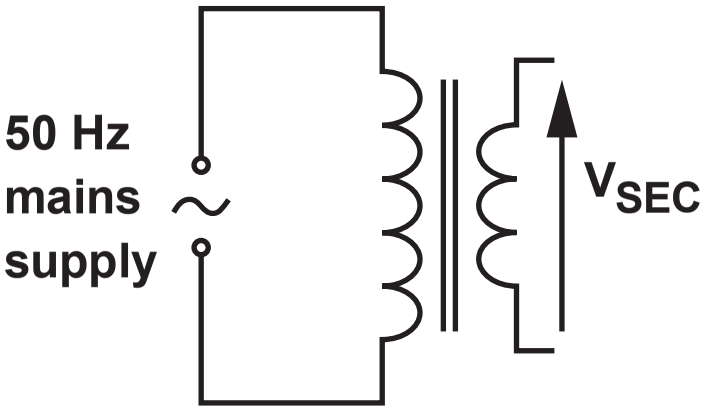
5. The diagram opposite shows an incomplete half-wave rectified power supply circuit.

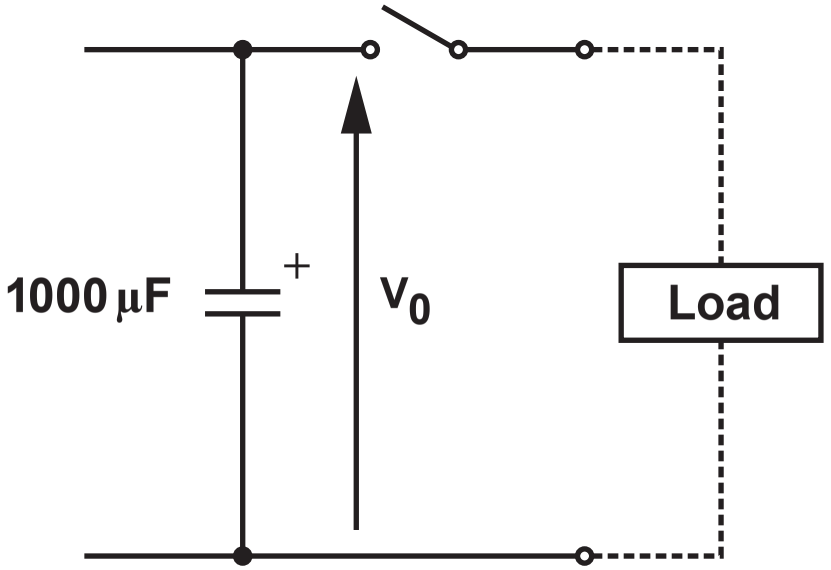
(a) (i) The PEAK value of the transformer secondary voltage, V_{SEC}, is 21.2 V.

Calculate the rms value of V_{SEC}. [2]

(ii) Complete the circuit diagram opposite. [2]

(iii) Calculate the peak voltage of the output voltage, V_0, when the switch is open. [1]

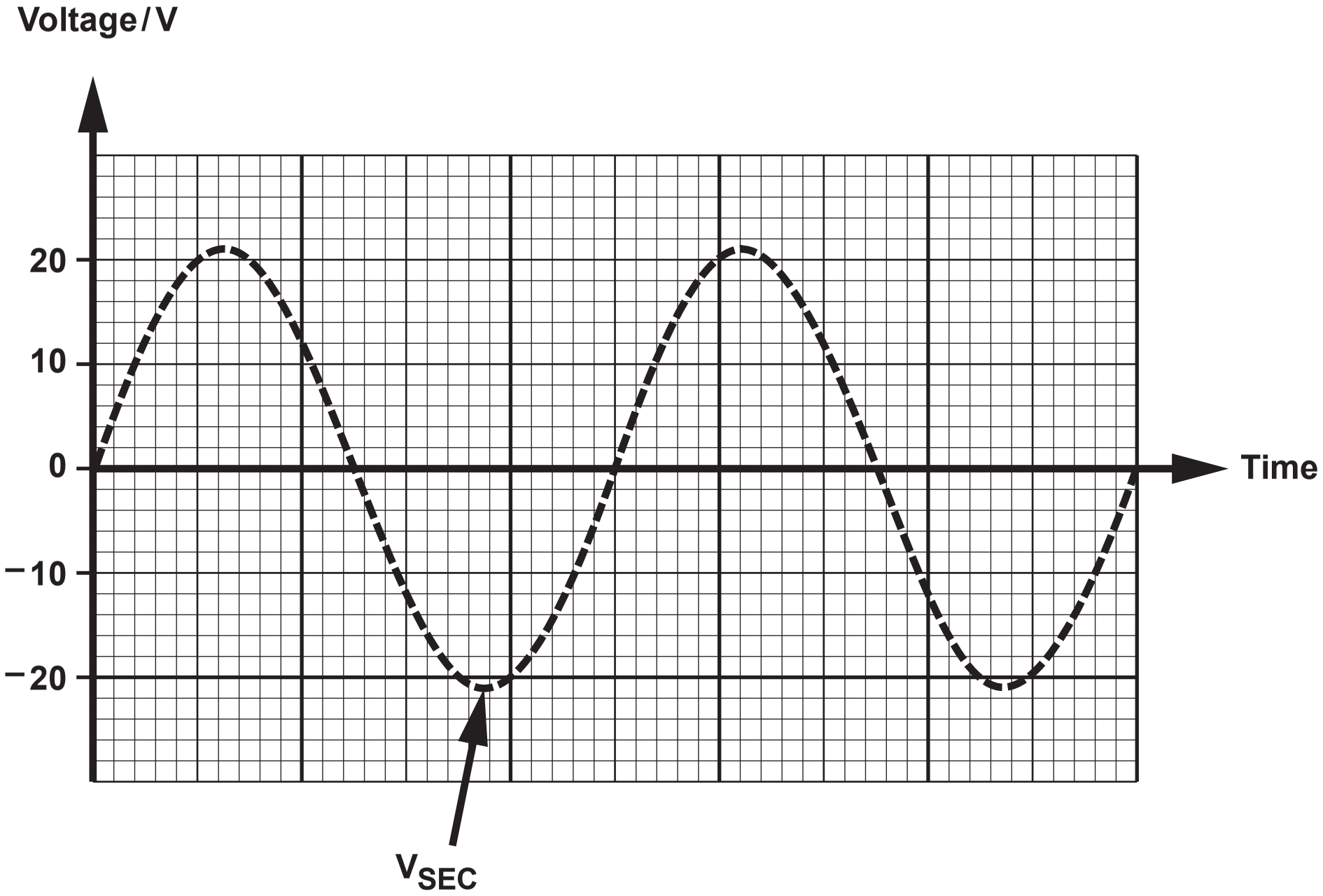

50 Hz
mains
supply
V_{SEC}


1000 μF
+
V_0
Load

5(a) (iv) **Calculate the ripple voltage when the load current is 0.2 A. [3]**

5(a) (v) **On the axes provided opposite, draw a graph of the voltage V_0 when there is a load current of 0.2 A. [3]**

The voltage, V_{SEC}, across the transformer secondary is shown as a dashed line.


Voltage / V
20
10
0
−10
−20
Time
V_{SEC}

5(b) **By modifying the power supply as shown opposite, it provides improved line regulation and some load regulation. It uses a 7.5 V zener diode.**

(i) **Complete the definitions for line and load regulation: [2]**

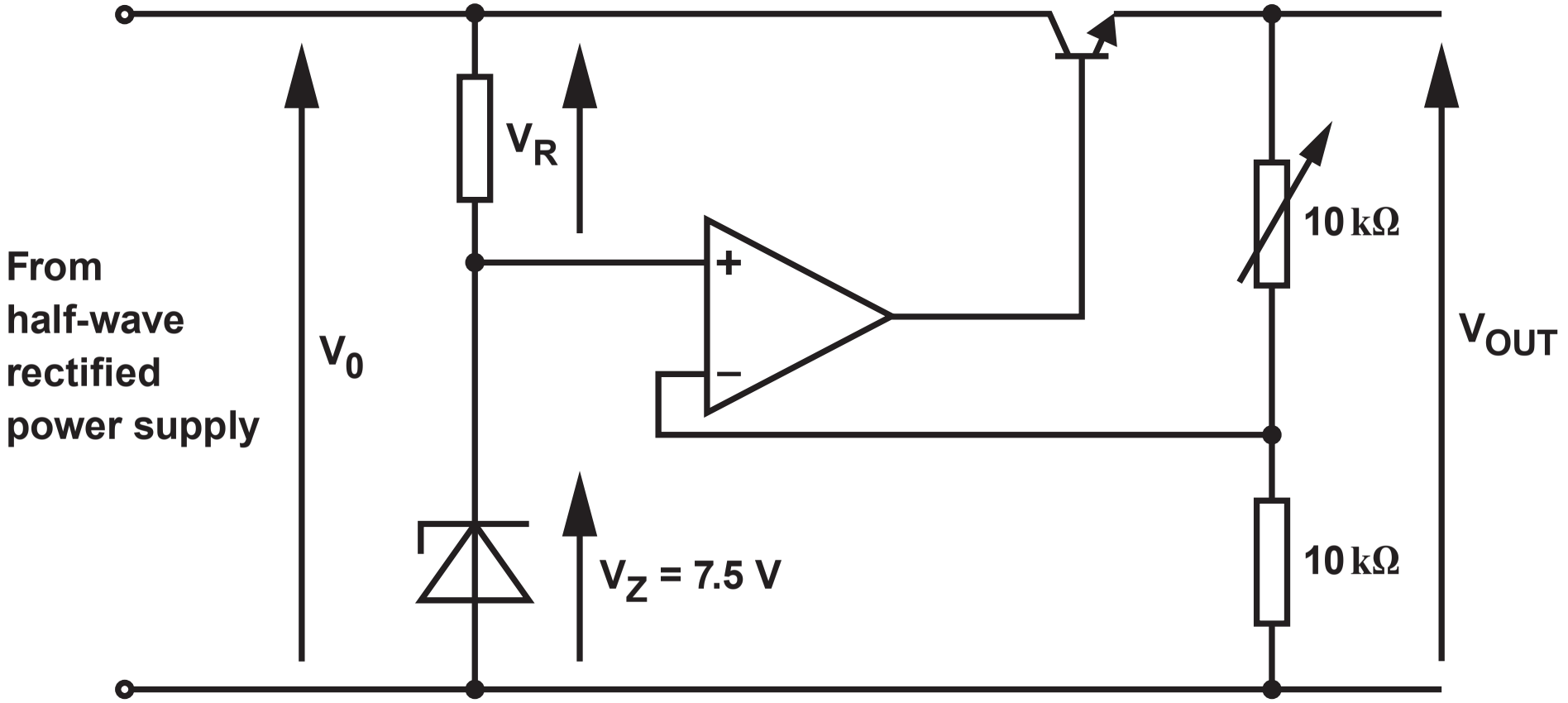
Line regulation means that the output voltage of the power supply remains unchanged when

---

Load regulation means that the output voltage of the power supply remains unchanged when

---

(ii) **Write an equation linking the quantities V_R, V_Z and V_0. [1]**


From
half-wave
rectified
power supply
V_0
V_R
+
−
V_Z = 7.5 V
10 kΩ
10 kΩ
V_{OUT}

5(b) (iii) Explain how this circuit delivers line regulation. [2]

5(b) (iv) **Calculate the maximum and minimum values of V_{OUT} obtained by adjusting the variable resistor. [3]**

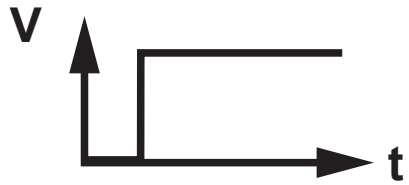
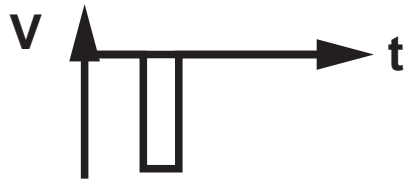
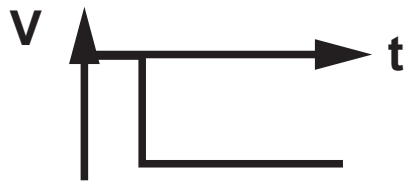
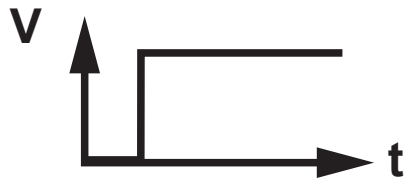
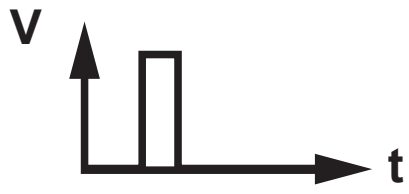
6(a) **The behaviour of a thyristor depends on the signal applied to the gate terminal and the voltage bias applied between its anode and cathode.**

The table opposite lists six combinations of these conditions, labelled A to F.

Select the two combinations which cause the thyristor to switch on. [2]

Combinations _____

and _____

	Input to gate	Bias
A		Reverse biased
B		Forward biased
C		Forward biased
D		Reverse biased
E		Forward biased
F		Reverse biased

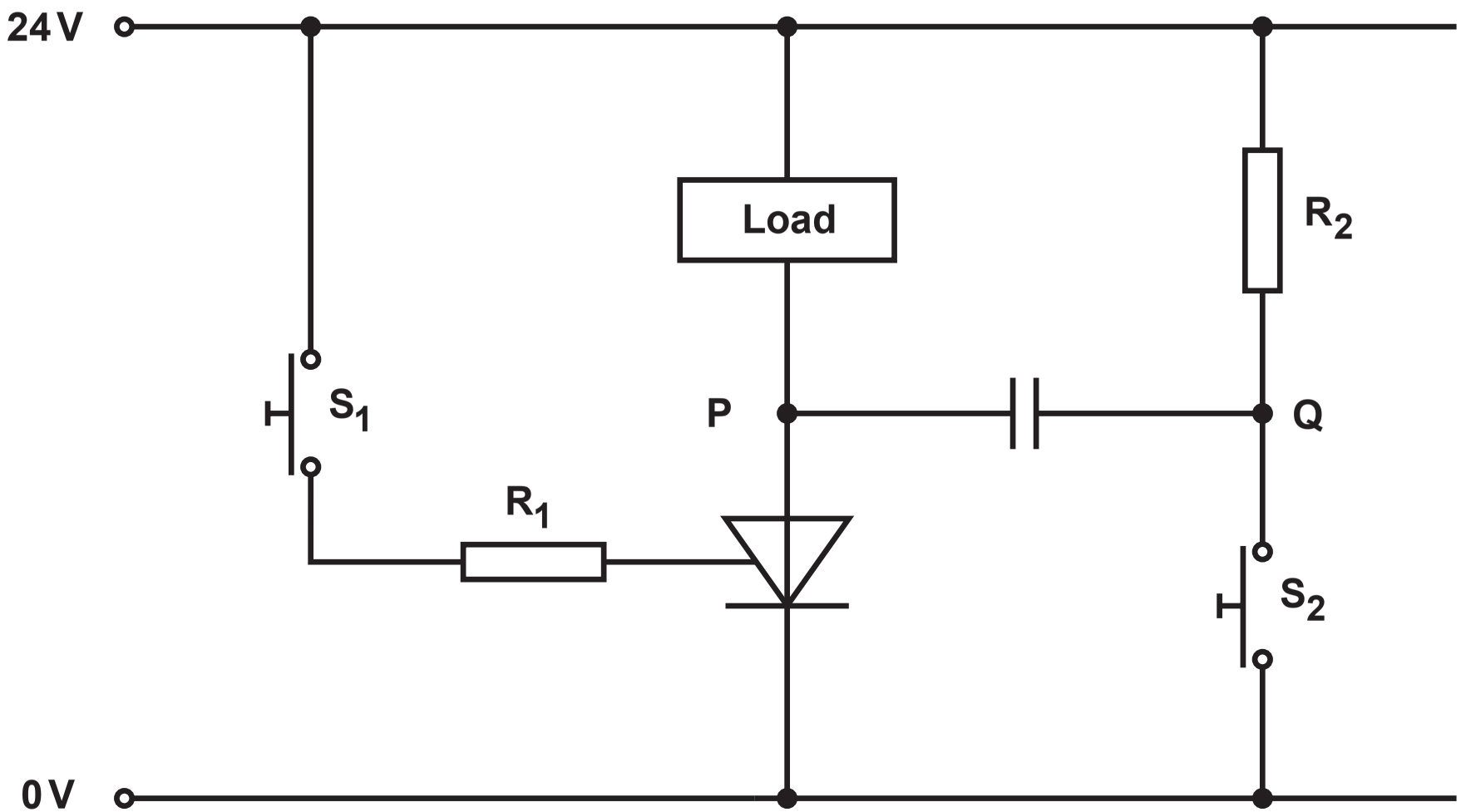
6(b) **A high-powered DC load is controlled by a thyristor.**

The circuit diagram for the control system is shown opposite.

(i) **Here is an extract from the data sheet for the thyristor:**

CHARACTERISTIC	VALUE
Minimum gate voltage	1.2 V
Holding current	200 mA
Minimum gate current	100 mA

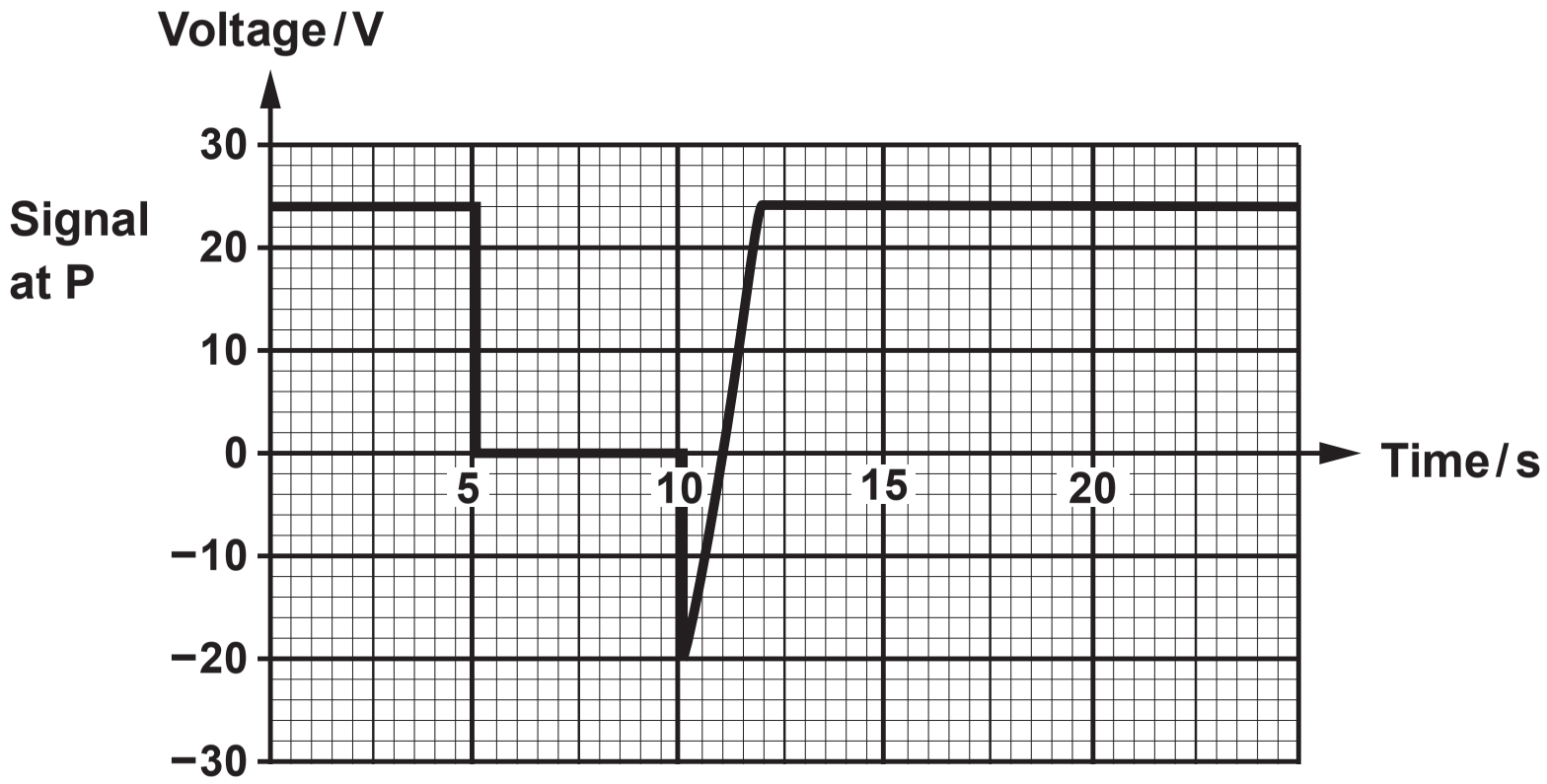
Calculate the maximum resistance for the resistor R_1. [3]

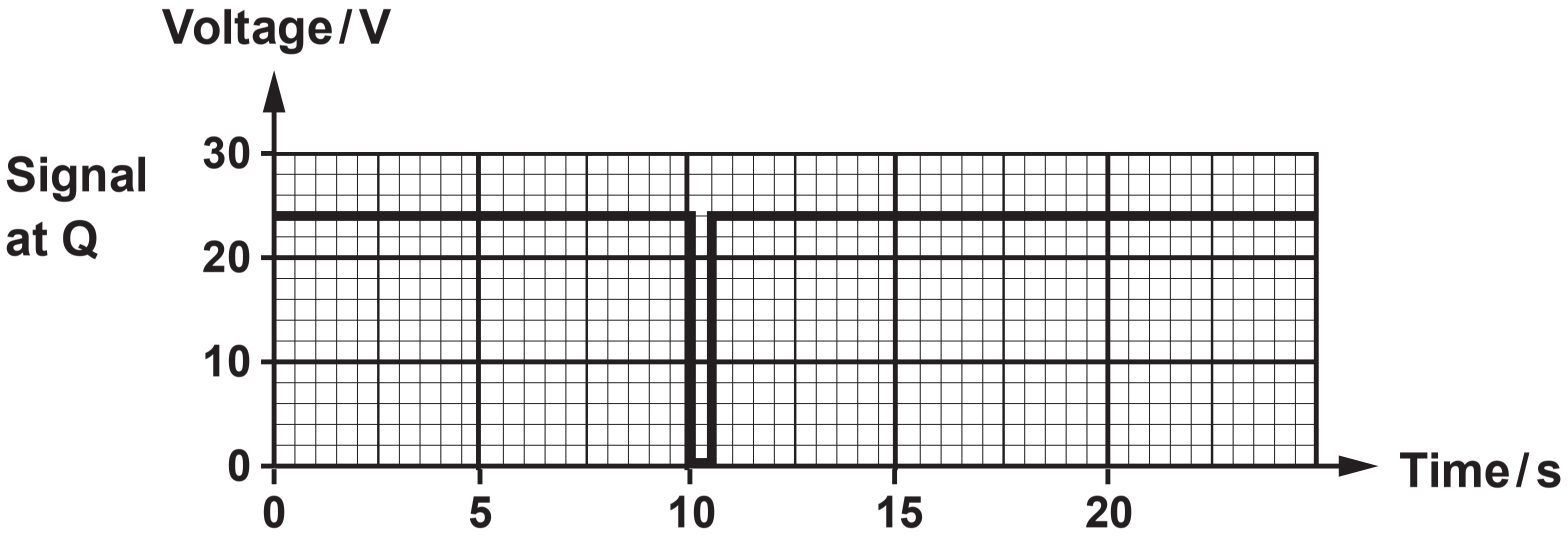

24 V
Load
R_2
S_1
P
Q
R_1
S_2
0 V

6(b) (ii) **The graphs opposite show the signals at points P and Q over a period of time:**

Explain what is happening to the switches and to the thyristor at:

- **time = 2 s; [2]**


Voltage / V
Signal at P
30
20
10
0
−10
−20
−30
5
10
15
20
Time / s


Voltage / V
Signal at Q
30
20
10
0
0
5
10
15
20
Time / s

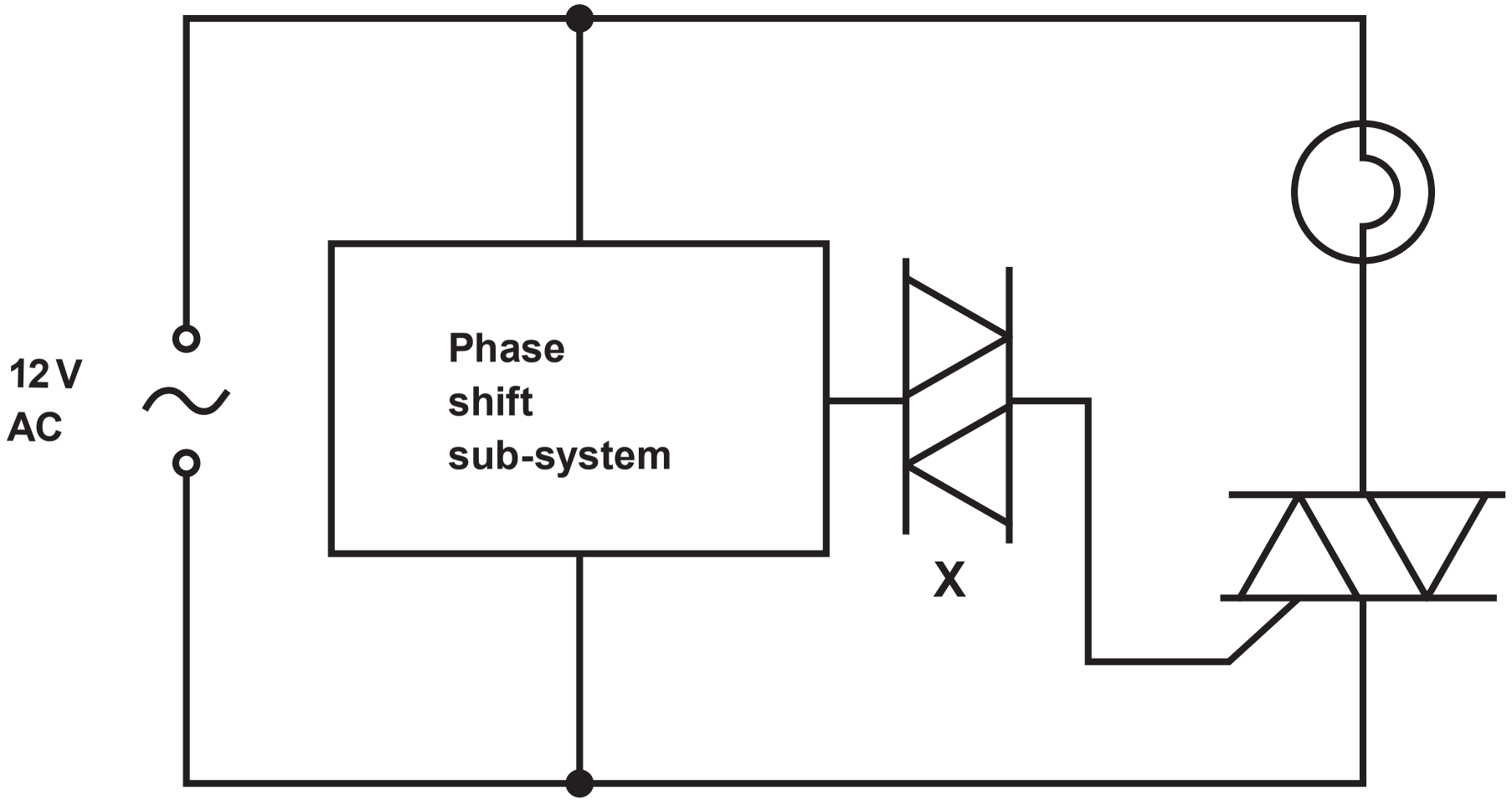
- **time = 5 s; [2]**

- **time = 10 s; [2]**

6(c) **A triac is used to control the brightness of a lamp, using a phase control sub-system.**

The circuit diagram is shown opposite:

(i) **Identify component X and describe its function in this system [2]**


12 V
AC
Phase
shift
sub-system
X

6(c) (ii) **The graph opposite shows the signal obtained at one point in the circuit:**

I. **Which component does this signal appear across? _____ [1]**

II. **Explain what is happening to the triac and to the lamp:**

between points P and Q; [1]

_____

_____

_____

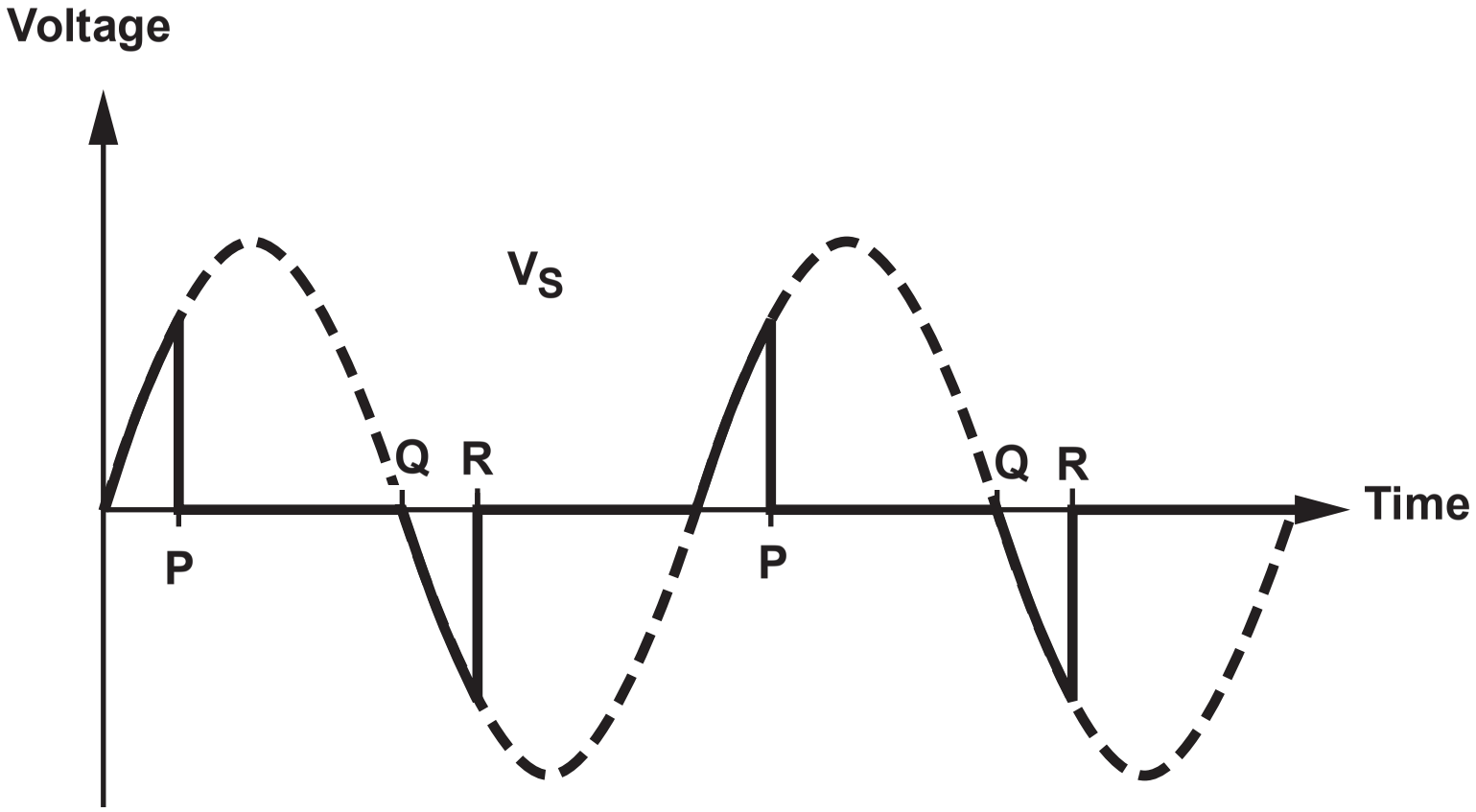
_____

_____

_____

_____

_____

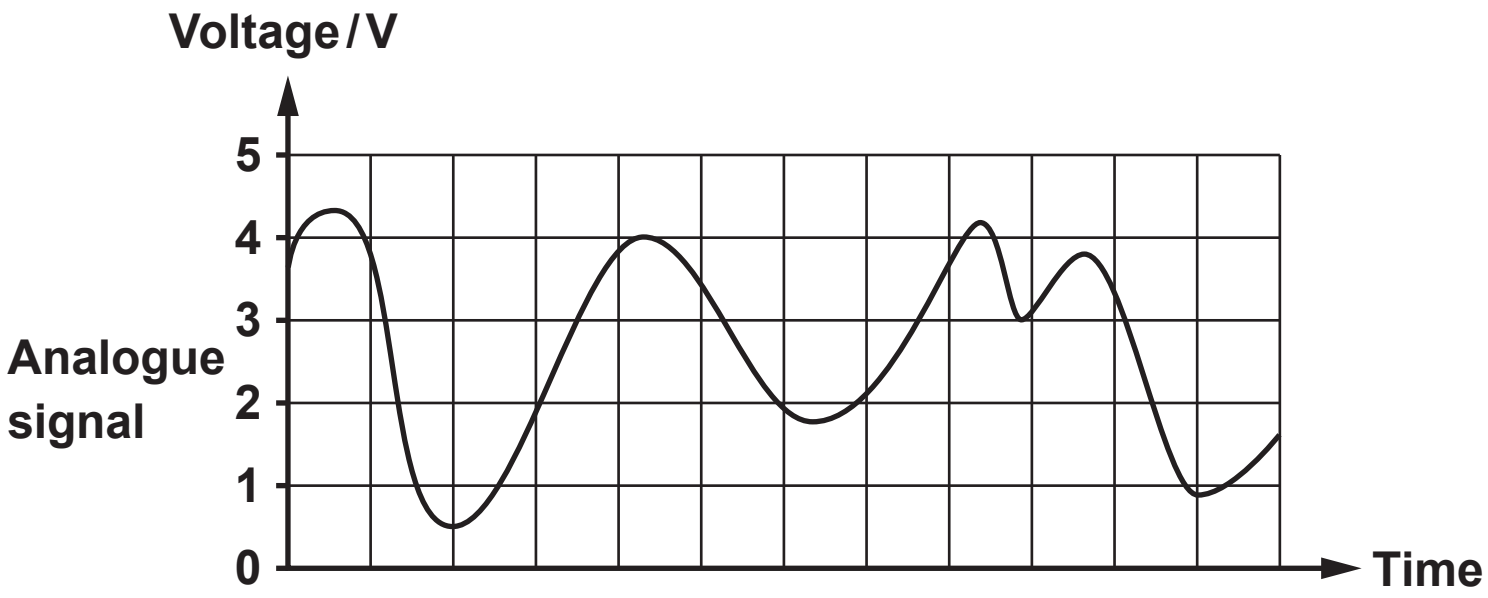

Voltage
V_S
Q
R
Q
R
Time
P
P

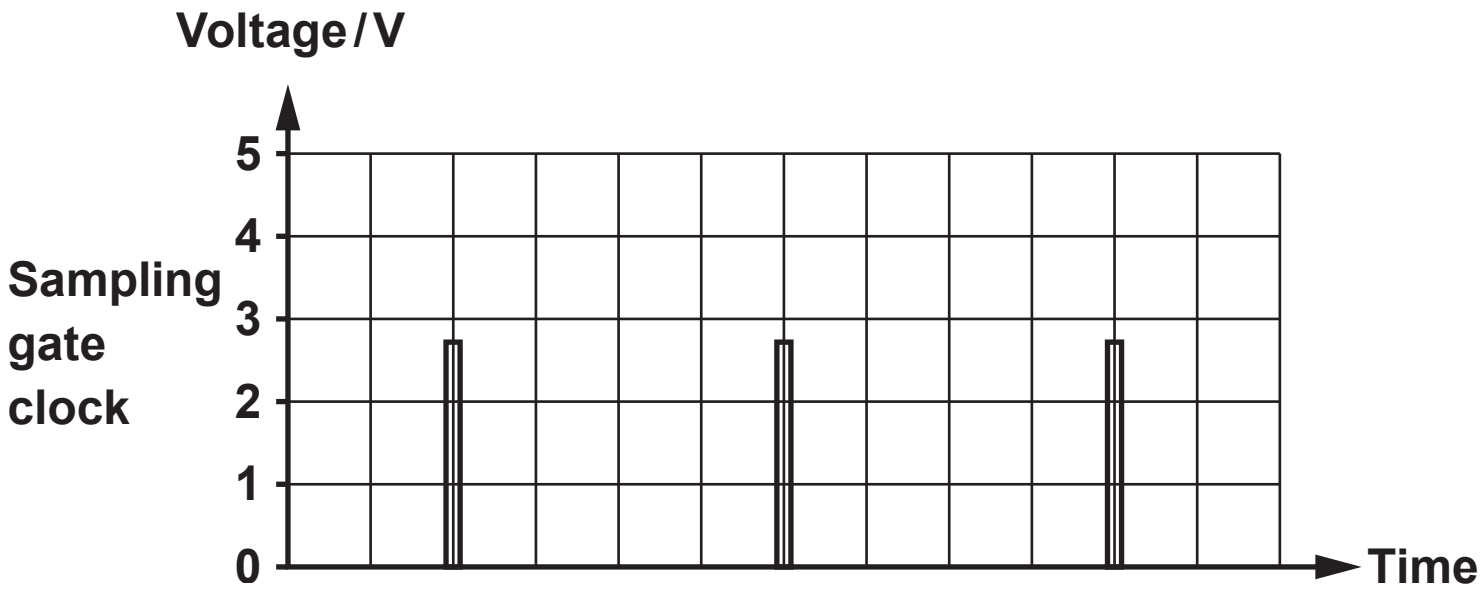
6(c)(ii) II. between points Q and R; [1]

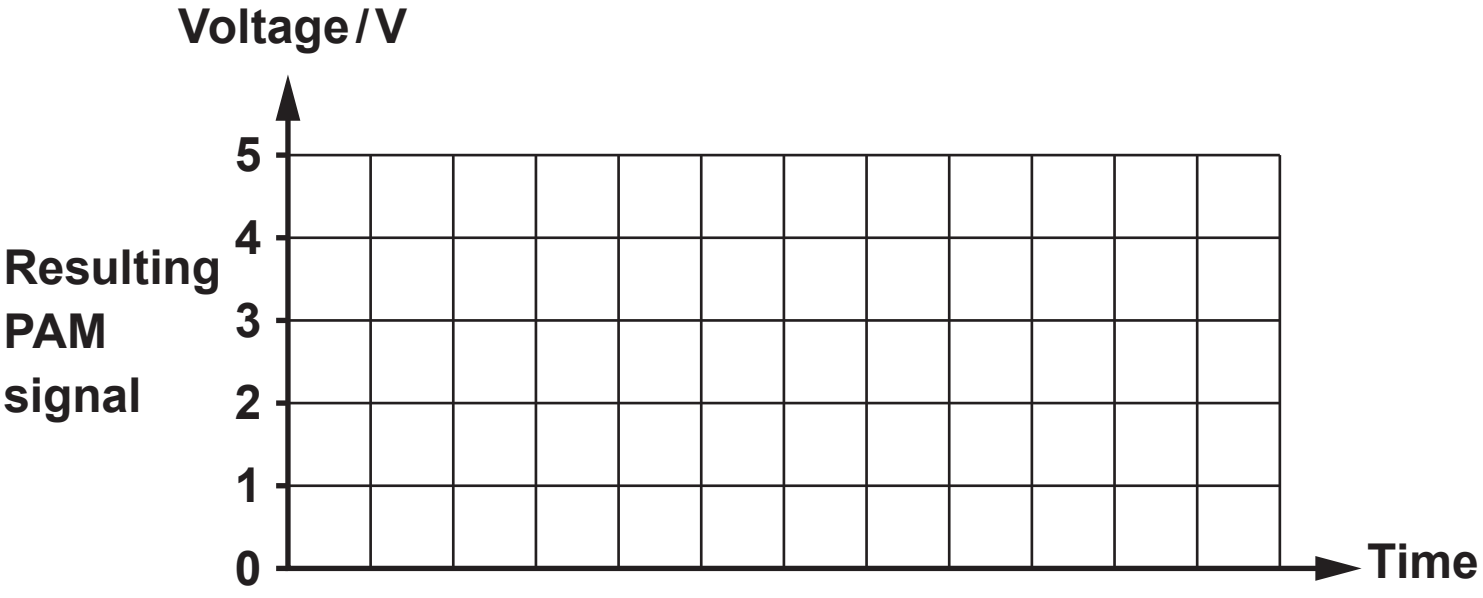
7(a) **Pulse-code modulation (PCM) is used to convert a signal from analogue into digital format, which can then be transmitted over a digital communication system.**

The first part of the process is to sample the analogue signal to produce pulse-amplitude modulation (PAM).

Complete the third graph opposite to illustrate this process for the given analogue signal and pulse train. **[2]**


Voltage / V
5
4
3
2
1
0
Analogue signal
Time


Voltage / V
5
4
3
2
1
0
Sampling gate clock
Time


Voltage / V
5
4
3
2
1
0
Resulting PAM signal
Time

7(b) Complete the block diagram opposite for a PCM RECEIVER, using the following sub-systems:

- **clock;**
- **DAC;**
- **low pass filter;**
- **Schmitt trigger;**
- **SIPO shift register. [4]**

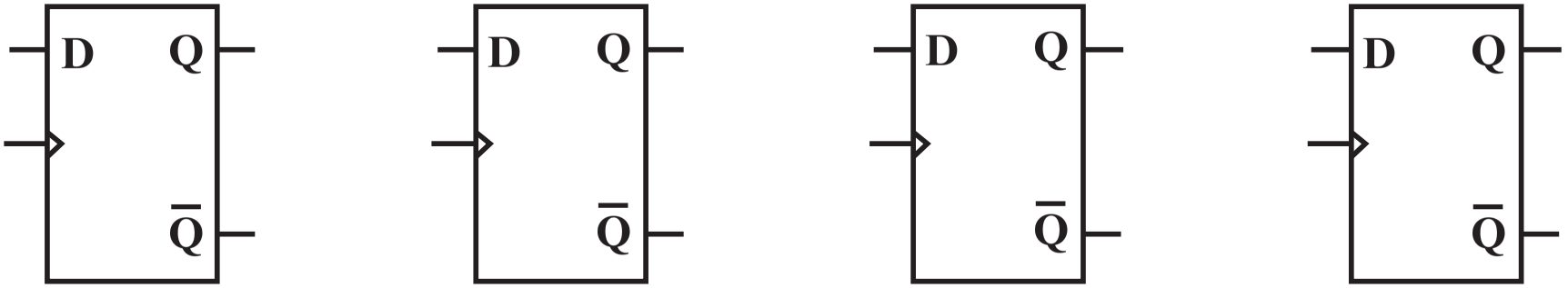

PCM
input
Analogue
output

7(c) (i) **Complete the circuit diagram opposite for a 4-bit serial-in-parallel out (SIPO) shift register based on D-type flip-flops.**

Data is inputted starting with the most-significant bit (msb).
Label:

- **the most-significant bit (msb) of the output, D;**
- **the least-significant bit (lsb) of the output, A;**
- **the serial input of the shift register.**

[3]

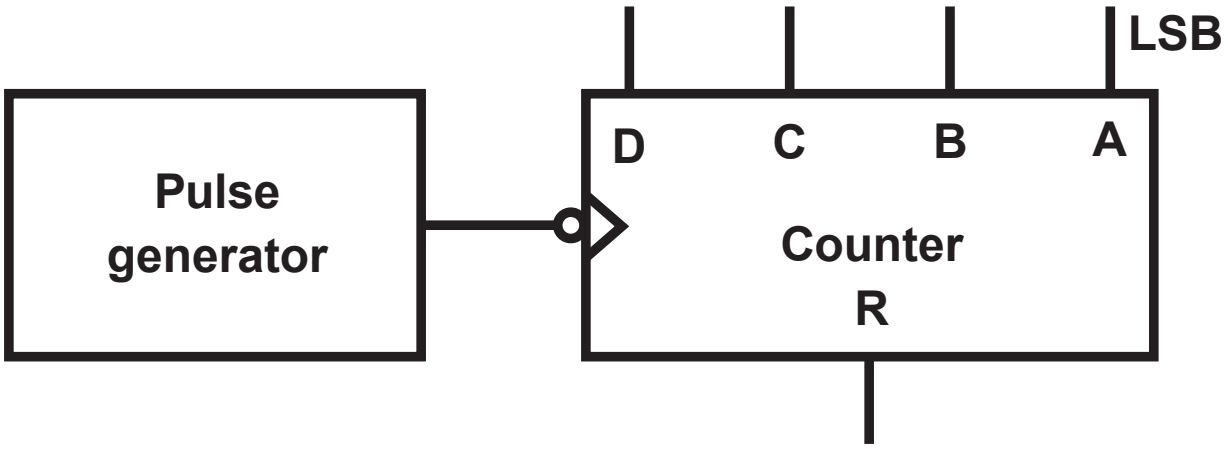

D
Q
$\overline{Q}$
D
Q
$\overline{Q}$
D
Q
$\overline{Q}$
D
Q
$\overline{Q}$

7(c) (ii) **The shift register is reset so that outputs A, B, C, and D are logic 0. A logic 1 signal is maintained at the serial input.**

Complete the table opposite to show the state of the outputs as four clock pulses are applied. [2]

	SERIAL INPUT	A	B	C	D
Reset	1	0	0	0	0
After one clock pulse	1				
After two clock pulses	1				
After three clock pulses	1				
After four clock pulses	1				

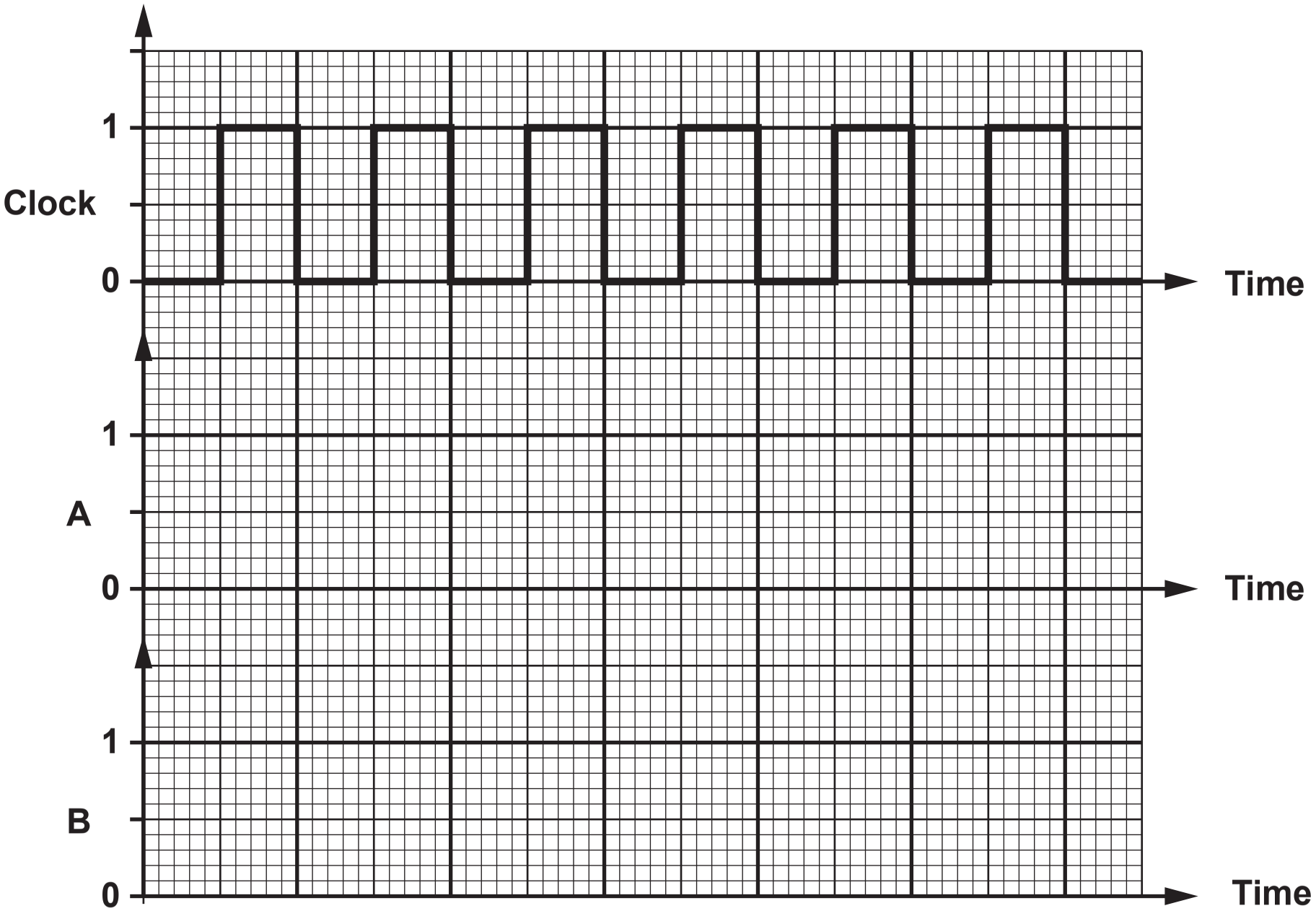
8(a) The following circuit diagram shows a dedicated 4-bit asynchronous (ripple) counter.



8(a) (i) Distinguish between asynchronous (ripple) counters and synchronous counters. [2]

8(a) (ii) **The counter is falling-edge triggered and is initially reset.**

Complete the timing diagram opposite to show the effect of the subsequent six clock pulses on counter outputs B and A. [3]

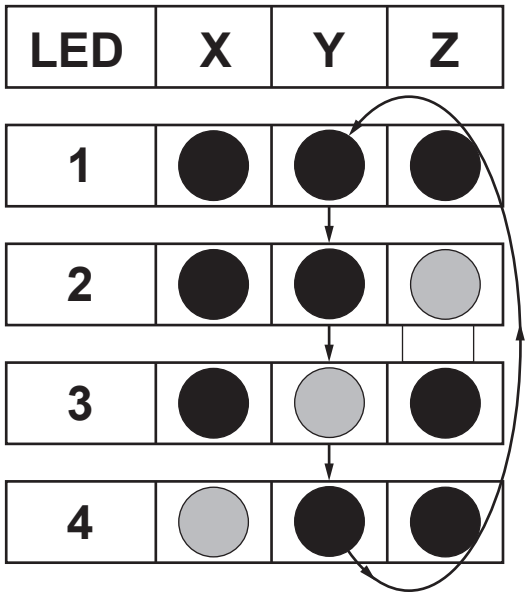

1
Clock
0
Time
1
A
0
Time
1
B
0
Time

8(b) **A system based on a dedicated 4-bit counter and combinational logic system is required to produce the following light sequence:**

Key

LED on

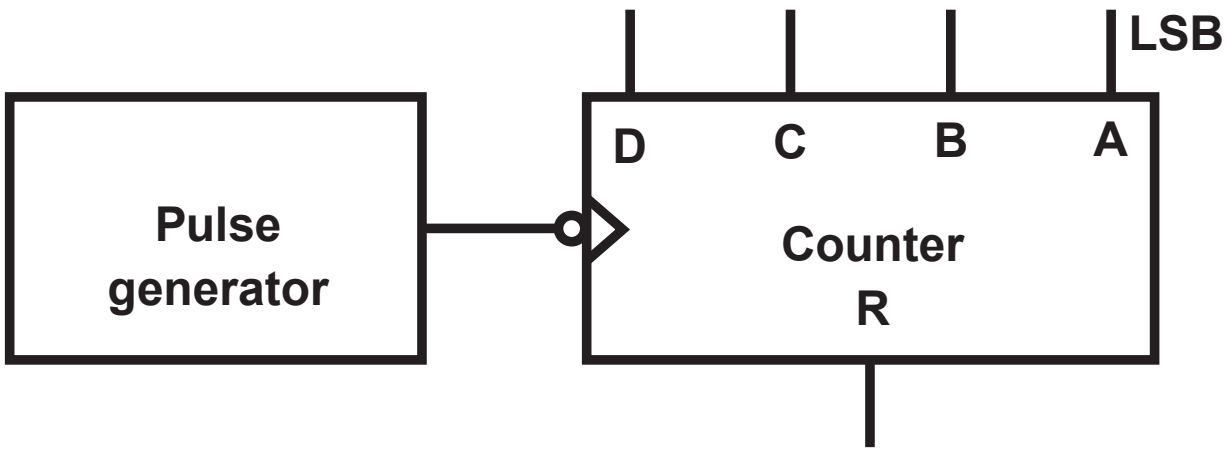
LED off



8(b) Design the system by completing:

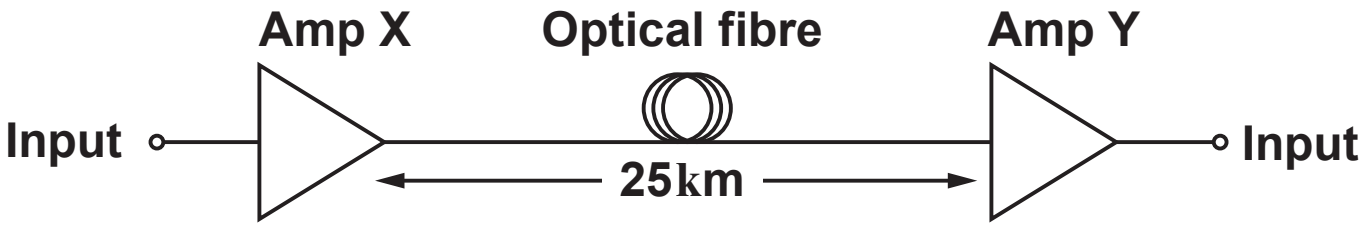
- **the truth table; [2]**
- **Boolean expressions for the outputs X, Y and Z; [3]**
- **the circuit diagram for the system opposite. [4]**

C	B	A	X	Y	Z
0	0	0	0	0	0


LSB
D
C
B
A
Pulse
generator
Counter
R

9(a) **Digital data is transmitted to the head office of a bank from one of its branch offices via an optical fibre link. Amplifiers X and Y are used to boost the signal amplitude.**

Input power = 2.5 mW



Amplifiers X and Y both have a gain of +30 dB.

The optical fibre link has an attenuation of $2\ \text{dB km}^{-1}$ and is 25 km long.

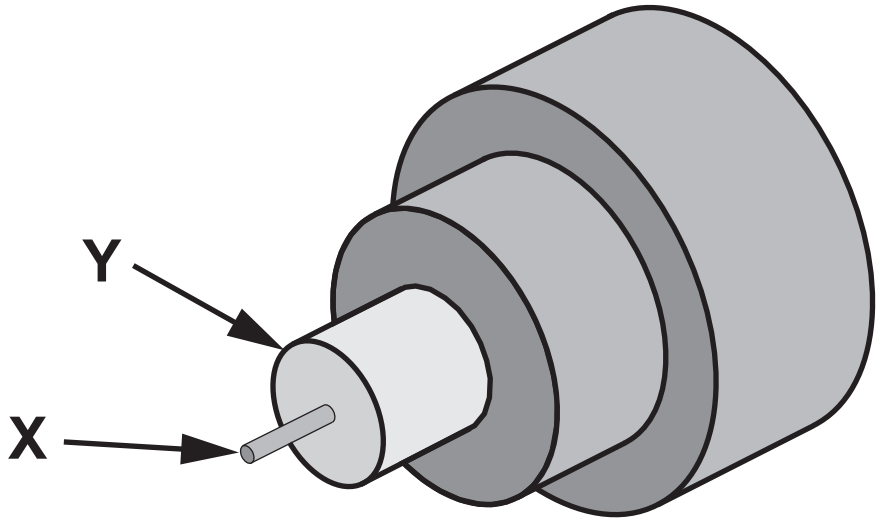
At the transmitter, the input power is 2.5 mW.

Calculate:

9(a) (i) the overall gain of the system in decibels; [2]

(ii) the output power in milliwatts; [2]

9(b) The diagram shows the typical structure of an optical fibre cable.



(i) Identify the components labelled X and Y. [2]

X = _____

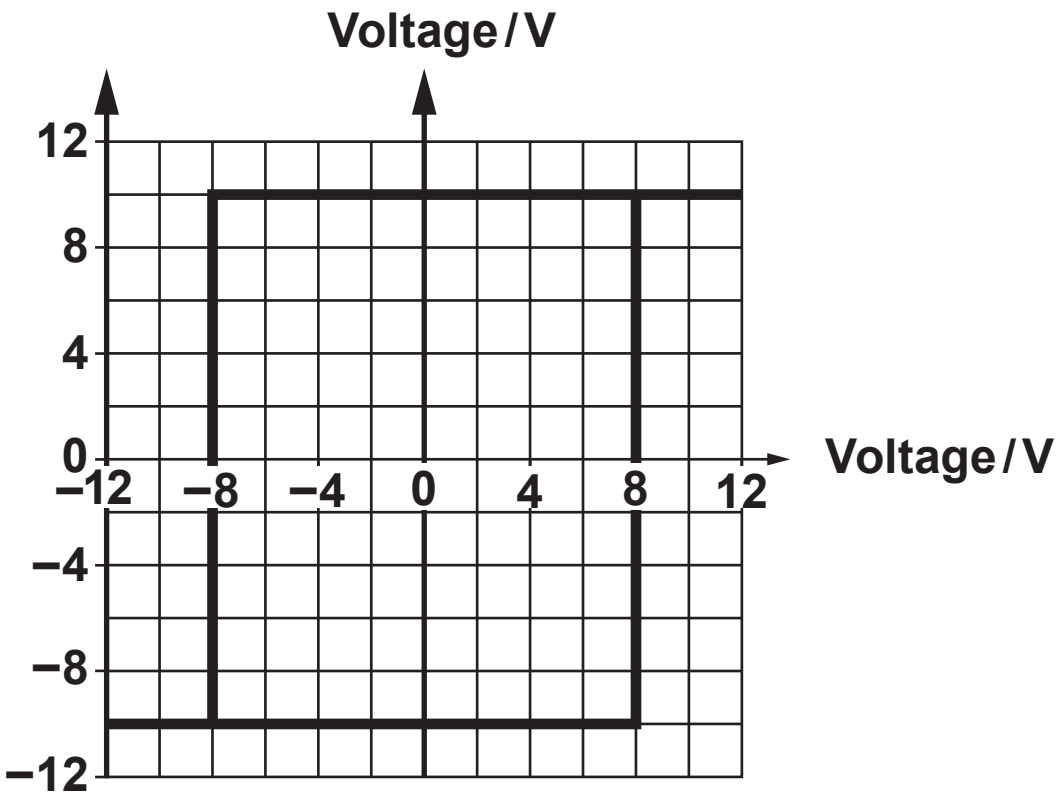
Y = _____

9(b) (ii) **The signal travels from amplifier X to amplifier Y using total internal reflection.**

Describe two conditions necessary for this to occur in this fibre. [2]

9(c) **The signal received at the output is converted back to an electrical signal, which is then regenerated by a Schmitt trigger sub-system.**

The graph opposite shows the characteristics for this Schmitt trigger.

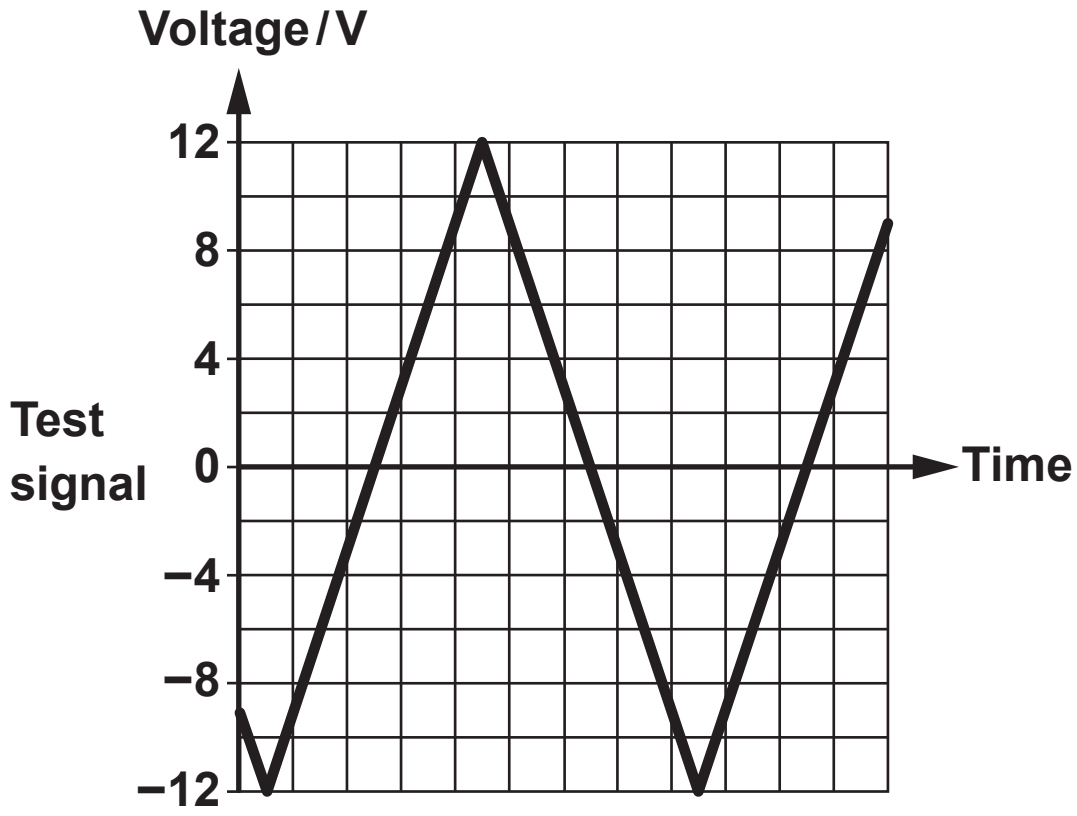

Voltage / V
12
8
4
0
−12
−8
−4
0
4
8
12
Voltage / V
−4
−8
−12

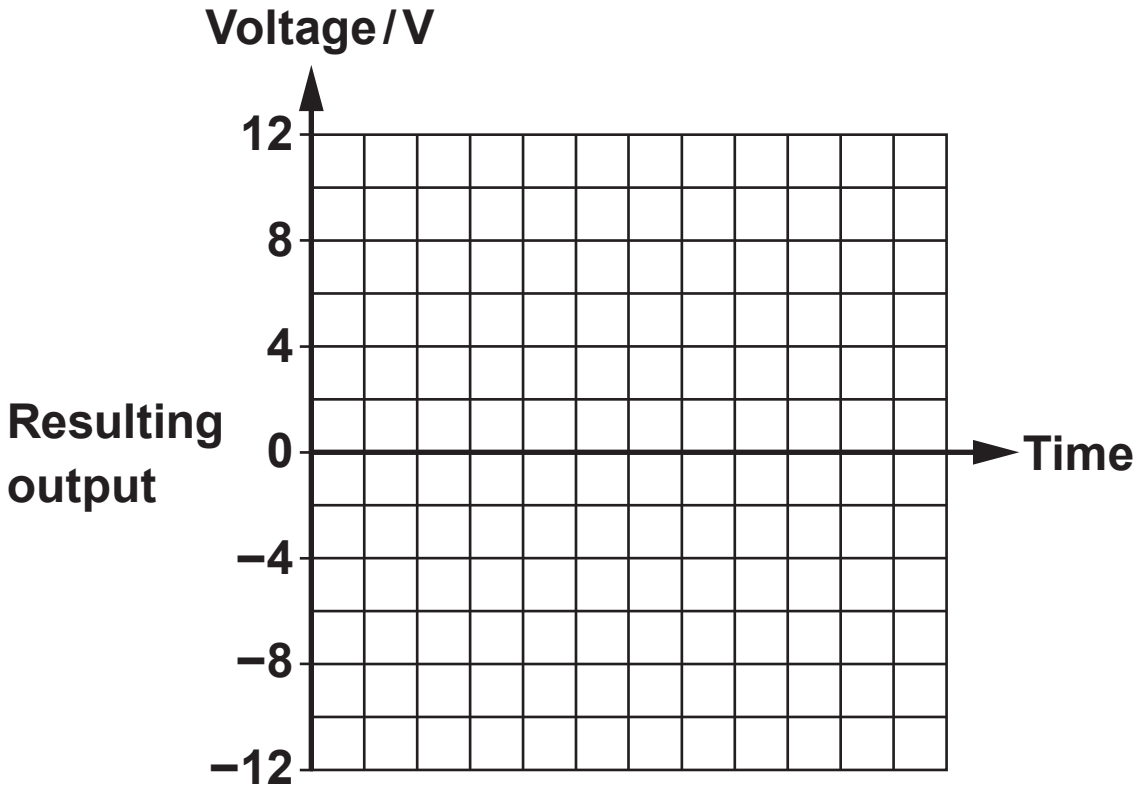
9(c) (i) **Design a Schmitt trigger circuit, based on a single op-amp, that has the characteristic as shown opposite page 56. [5]**

Draw the circuit diagram for your design in the space below.

9(c) (ii) **Complete the second graph opposite to show the effect of this Schmitt trigger on the signal given in the first graph. [3]**

END OF PAPER


Voltage / V
12
8
4
0
−4
−8
−12
Test signal
Time


Voltage / V
12
8
4
0
−4
−8
−12
Resulting output
Time