GCE A LEVEL

A490U20-1

FRIDAY, 9 JUNE 2023 – AFTERNOON

ELECTRONICS – A level component 2

Application of Electronics

2 hours 45 minutes plus your additional time allowance

Surname _____

First name(s) _____

Centre Number _____

Candidate Number 2 _____

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	10	
2.	18	
3.	13	
4.	16	
5.	6	
6.	14	
7.	19	
8.	16	
9.	12	
10.	16	
Total	140	

ADDITIONAL MATERIALS

You will require a calculator and a DATA BOOKLET.

INSTRUCTIONS TO CANDIDATES

Use black ink, black ball-point pen or your usual method.

You may use a pencil for graphs and diagrams only.

Write your name, centre number and candidate number in the spaces provided on the front cover.

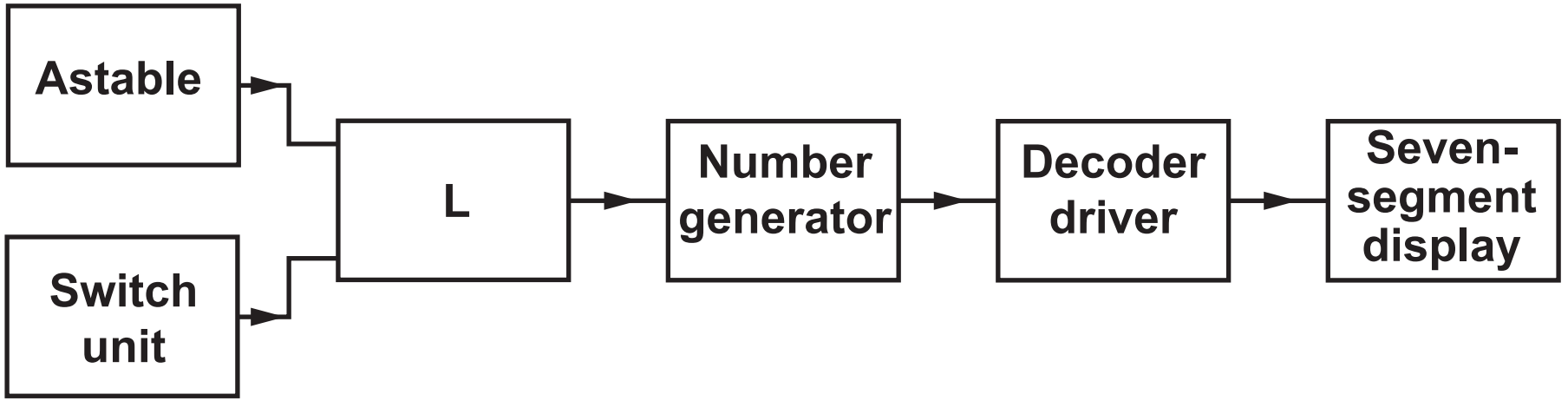
Answer ALL questions.

Write your answers in the spaces provided in this booklet. If you run out of space, use the additional page(s) at the back of the booklet, taking care to number the question(s) correctly.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in question 5.


Astable
Switch unit
L
Number generator
Decoder driver
Seven-segment display

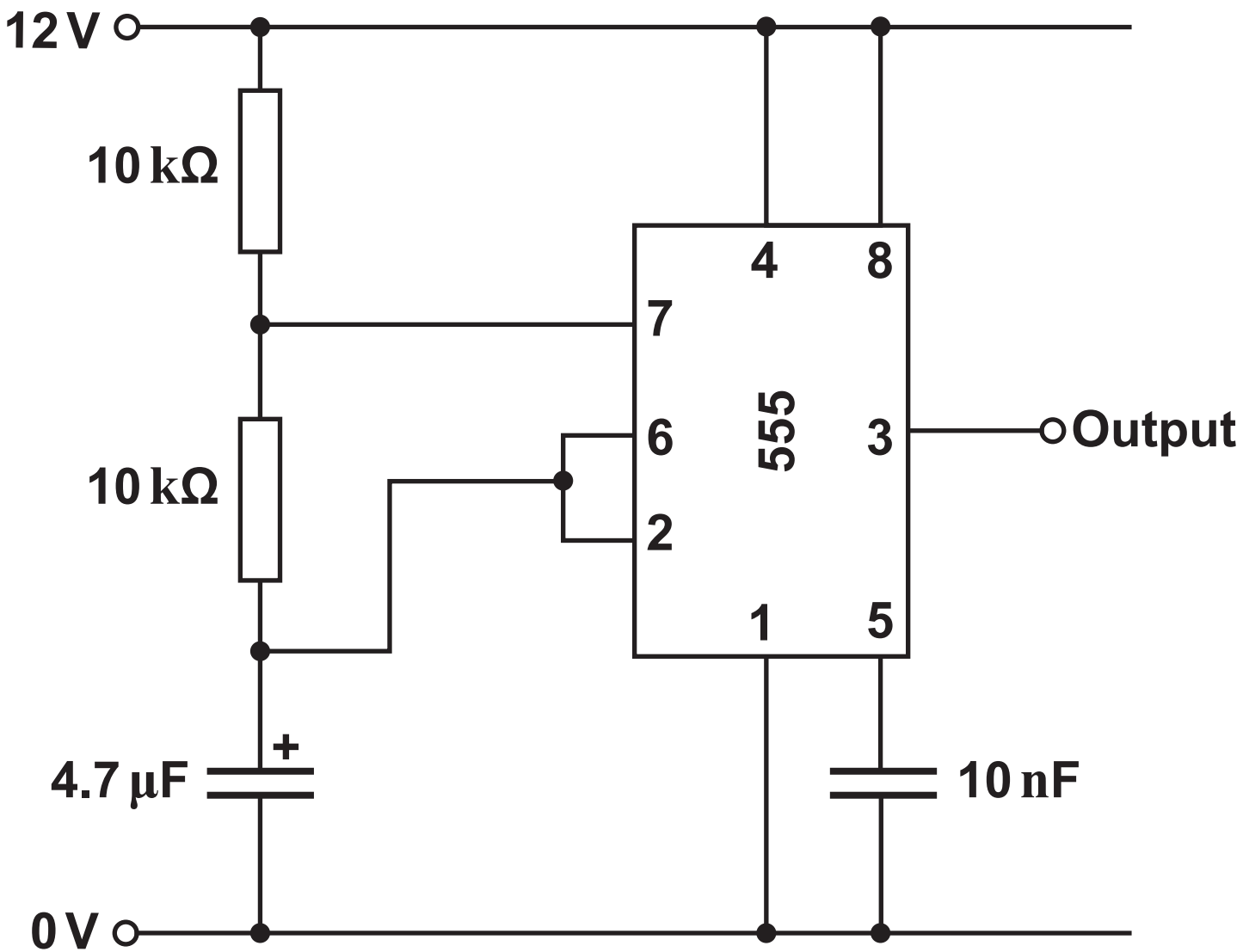
Answer ALL questions.

1. The block diagram for an electronic dice is shown opposite:

When the switch is closed, the switch unit outputs a logic 0 signal and the number generator then repeatedly runs quickly through the number sequence from '1' to '6'.

When the switch is then opened, the sequence stops and a fixed number is displayed.

(a) What type of logic gate must be used in block L in this system? [1 mark]

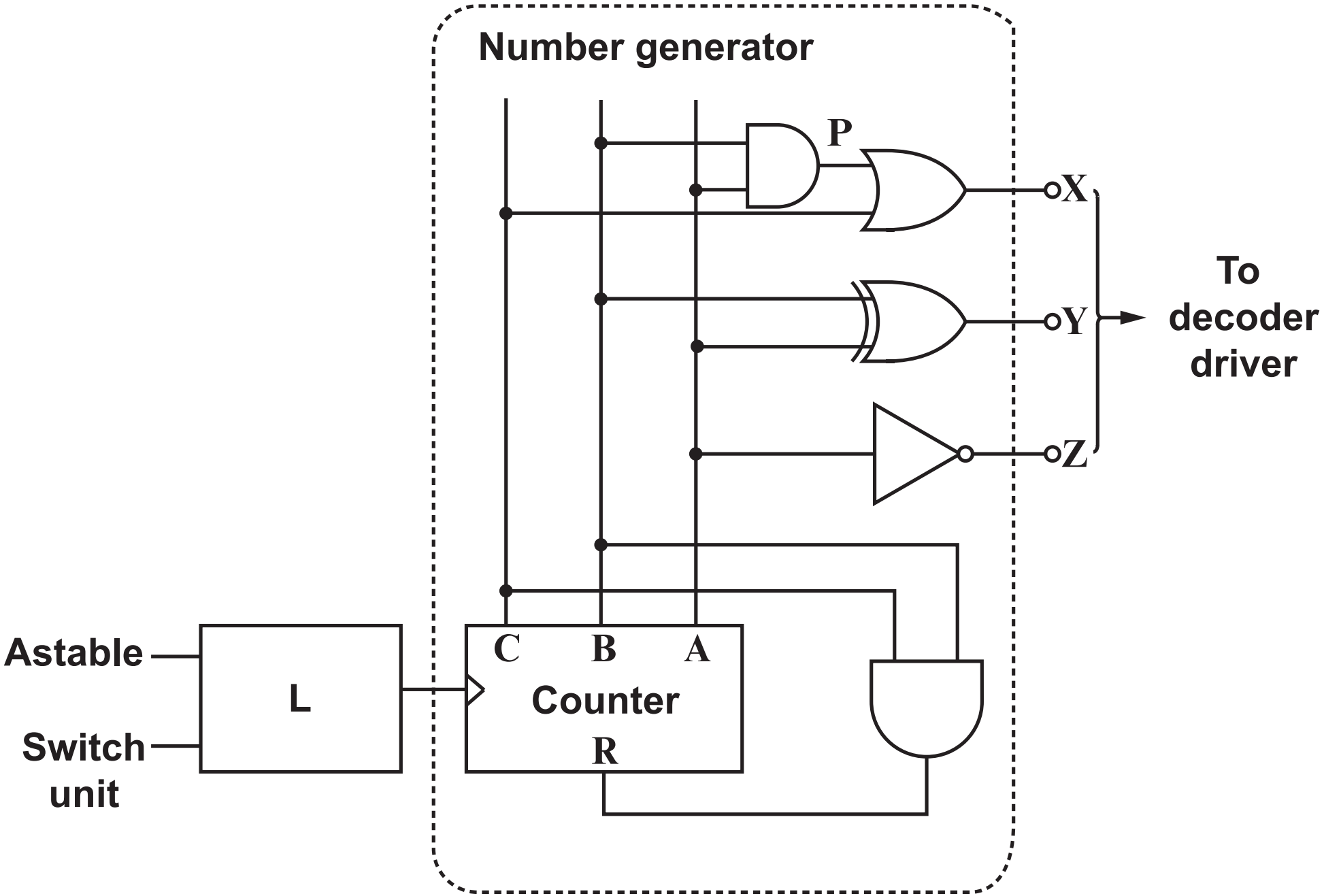

12 V
10 kΩ
10 kΩ
4.7 µF
+
0 V
4
8
7
6
555
3
2
1
5
Output
10 nF

1 (b) The astable uses a 555 timer IC. The circuit is shown opposite.

Calculate:

(i) the frequency of the astable; [2 marks]

(ii) the mark/space ratio of the pulse train produced. [2 marks]


Number generator
P
X
Y
Z
To
decoder
driver
Astable
Switch
unit
L
C
B
A
Counter
R

1 (c) A student designs the following counter and combinational logic system to generate the number sequence see diagram opposite.

Complete the truth table for the number generator.

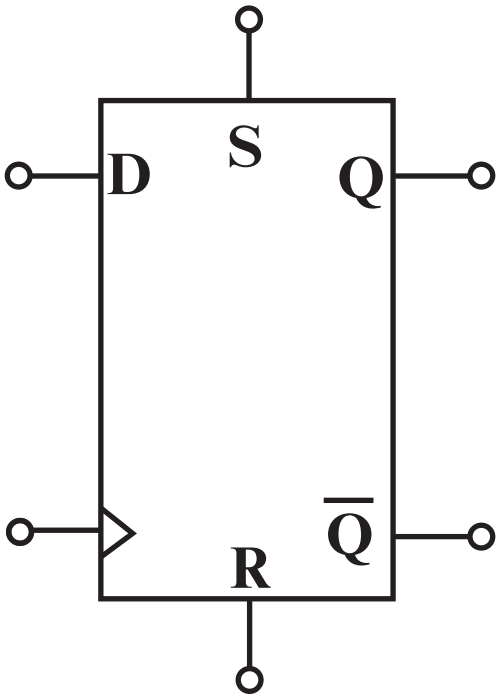
[5 marks]

C	B	A	P	X	Y	Z
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

10

2 (a) The diagram shows the symbol for a D-type flip-flop including Set (S) and Reset (R) inputs.

It is rising-edge triggered and the set and reset inputs are both active-high.



The graphs opposite show the signals applied to the inputs.

Complete the timing diagrams to show the resulting Q and $\overline{Q}$ outputs.

The Q output is initially at logic 0. [5 marks]

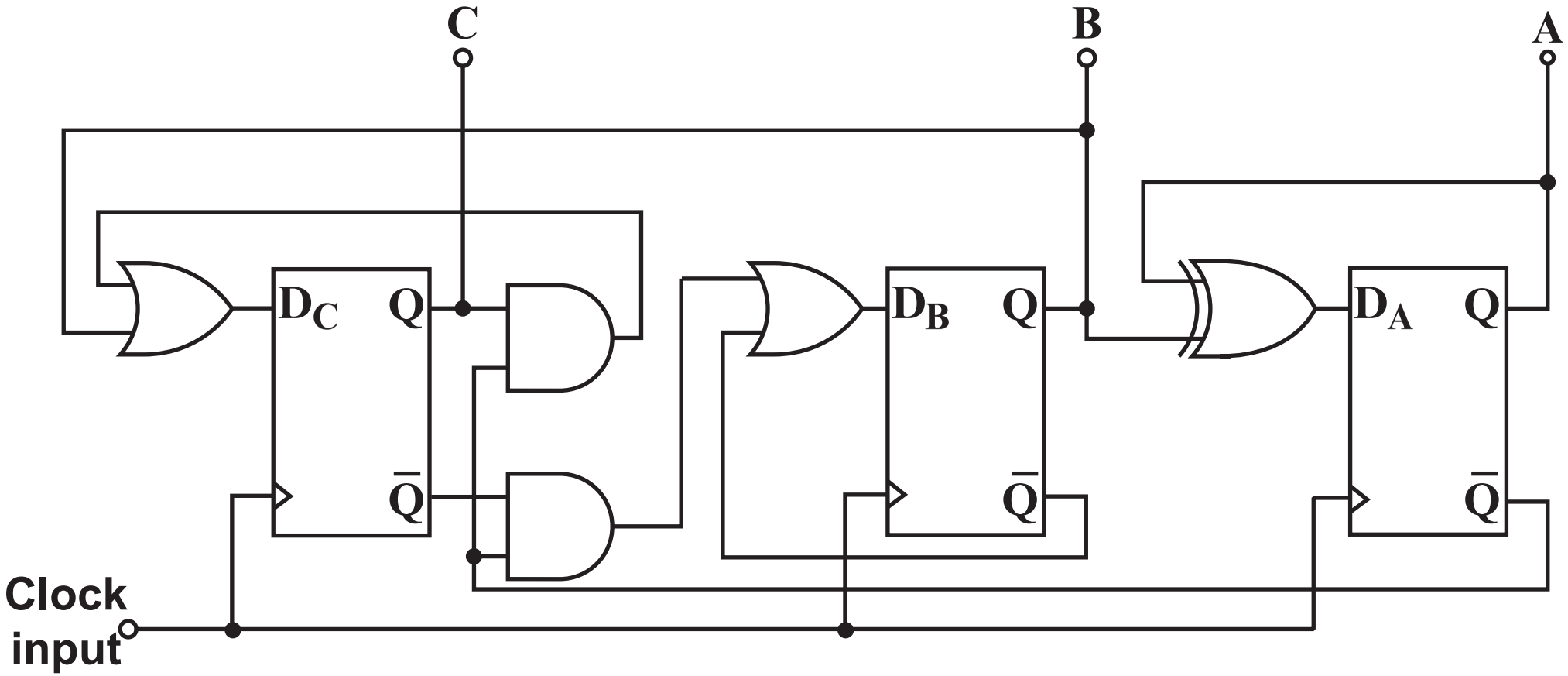
2 (b) Three D-type flip-flops are connected as a sequence generator.
(The set and reset inputs are not used and all are connected to 0 V.)

(i) Complete Boolean expressions linking the inputs D_C, D_B and D_A to outputs C, B and A. [5 marks]

D_C = _____

D_B = _____

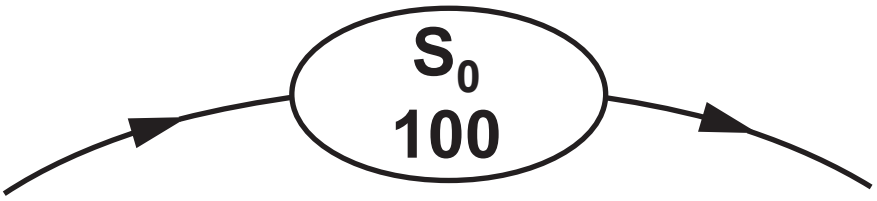
D_A = _____


C
B
A
D_C
Q
$\overline{Q}$
D_B
Q
$\overline{Q}$
D_A
Q
$\overline{Q}$
Clock input

2 (b) (ii)

Complete the truth table for the sequence generator. [4 marks]

Current state			Next state		
C	B	A	D_C	D_B	D_A
1	0	0			


S0
100

2 (b) (iii) Use the truth table opposite to determine the main sequence and unused states. Hence, draw the state diagram. [2 marks]

(iv) It is important that a sequence generator is designed to avoid stuck states.

What are stuck states and why must a sequence generator avoid them? [2 marks]

3. **A microcontroller is programmed to wait for a switch to be pressed and then light an LED for 3 s.**

It uses a switch unit which outputs a logic 1 signal when the switch is pressed.

The switch unit is connected to Port A bit 7 of a PIC 16F88 microcontroller. All other bits of Port A are set as outputs.

(a) **Complete the following instructions to set up Port A as described above. [3 marks]**

movlw b‘ _____’

_____ _____

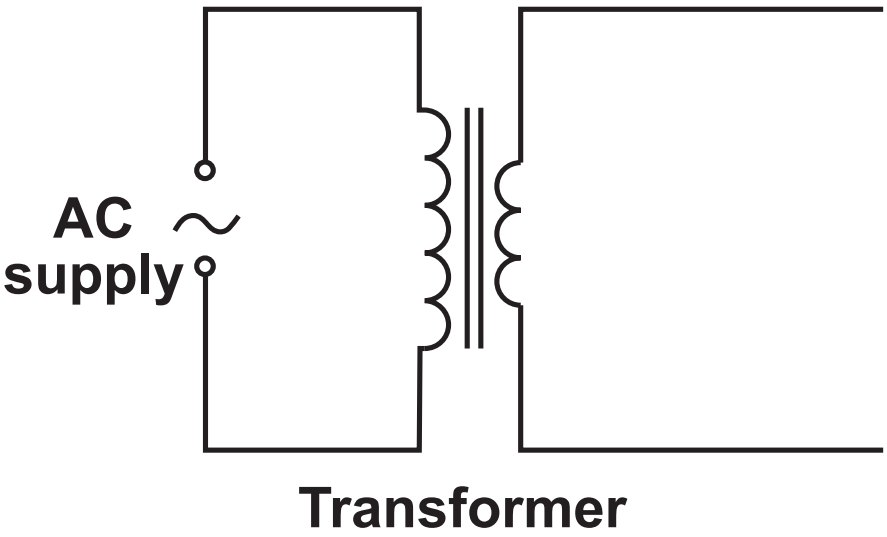
3 (b) An LED, connected to Port A bit 2, lights when it receives a logic 1 signal.

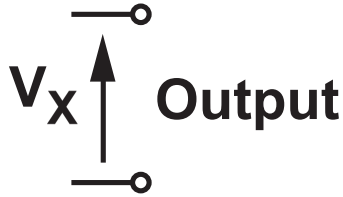
A delay subroutine, called onesec, is available. It creates a one second time delay.

Complete the following section of code on the opposite page that:

- waits for the switch to be pressed
- then lights the LED for three seconds
- then waits for the switch to be pressed again.

[10 marks]

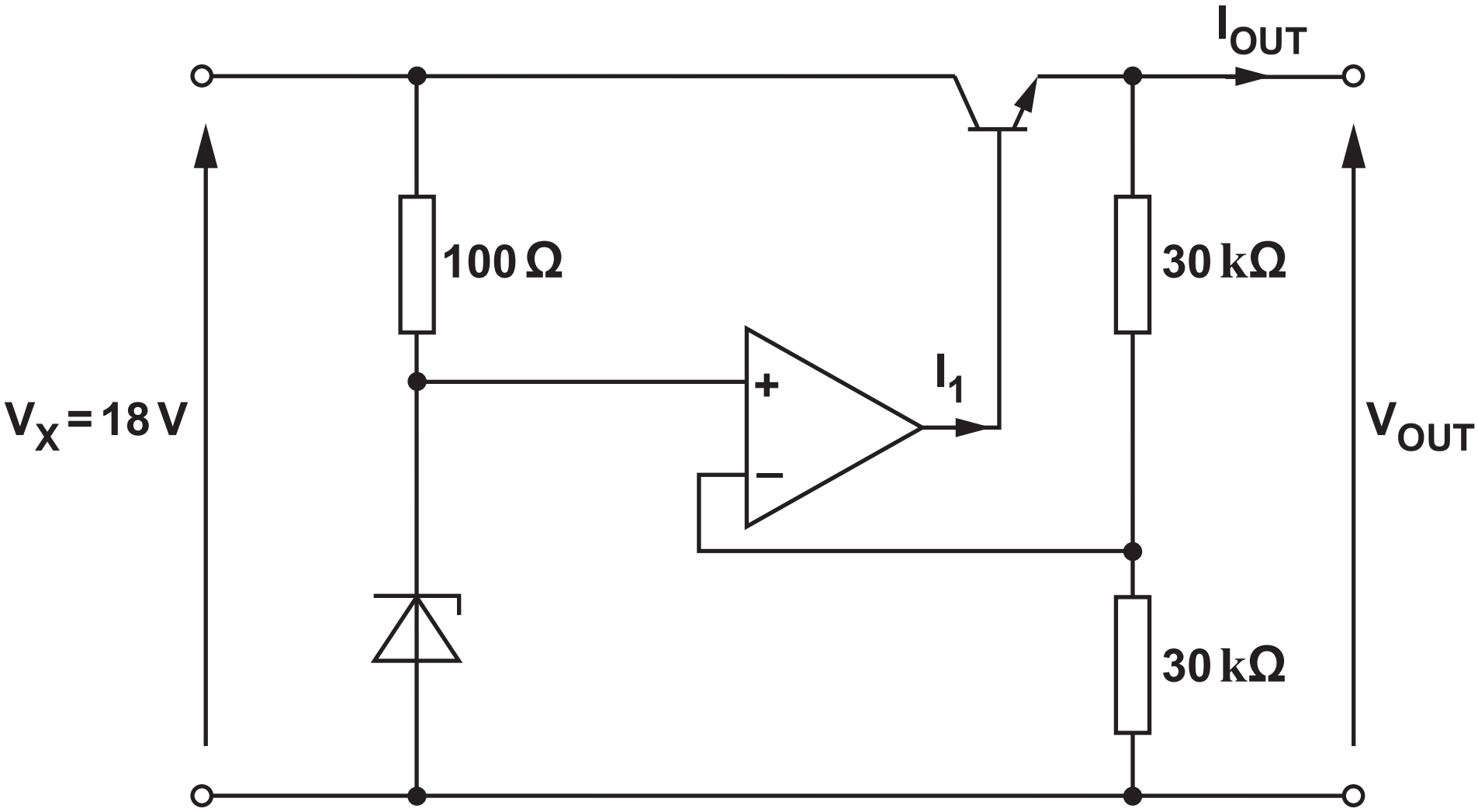

AC
supply
Transformer


V_X
Output

4 (a) Complete the diagram opposite for a smoothed full-wave rectifier. [3 marks]

(b) Power supplies often have good 'load regulation'. Explain what is meant by 'load regulation'.

[2 marks]


I_{OUT}
100 Ω
30 kΩ
I_1
+
–
$V_X = 18\,V$
V_{OUT}
30 kΩ

4 (c) **The circuit opposite is added to the output of this full-wave rectifier.**

(i) **The output voltage V_{OUT} = 15 V.**
Circle a suitable value of zener voltage from the list and justify your answer with a calculation. [3 marks]

Possible zener voltage values:

3 V 7.5 V 10 V 15 V 18 V

Justification:

4 (c) (ii)

The transistor has a current gain, h_{FE} of 40.
With a load connected the current I_{OUT} = 320 mA.
The currents flowing into the inputs of the op-amp are negligibly small.
Calculate the current I_1 delivered by the op-amp.

[2 marks]

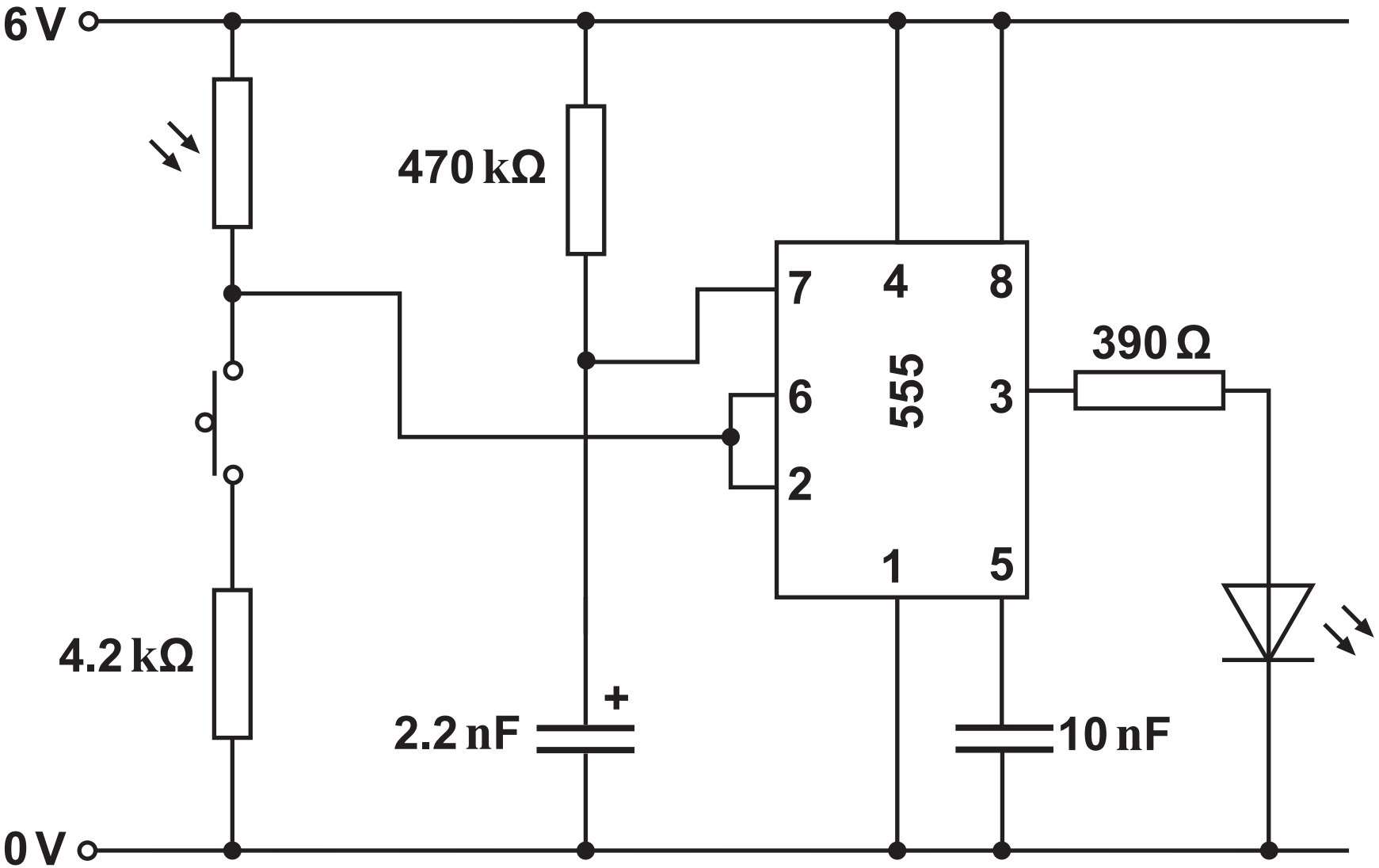
4 (c) (iii)

Calculate the power dissipated in the zener diode.

[3 marks]

4 (c) (iv)

Explain the role of the non-inverting amplifier in this power supply when the output voltage V_{OUT} starts to decrease. [3 marks]


6 V
470 kΩ
7
4
8
390 Ω
555
6
3
2
1
5
4.2 kΩ
2.2 nF
+
10 nF
0 V

5. **A student photographer wants a system that lights an LED when the light level is so low that additional lighting from a flash is needed.**

The specification for the system is as follows:

- **it runs off a 6 V battery**
- **an LED lights for one second if the light level is too low**
- **the system is triggered by a push switch provided that the light level is below 100 lux.**

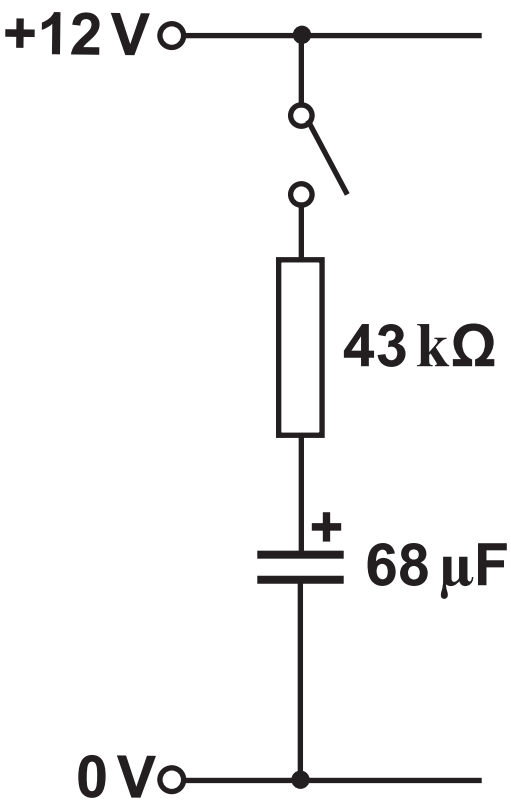
The following information is used in designing the system:

- **the LED passes a current of approximately 10 mA when lit and has a forward voltage drop of 2 V**
- **pin 2 of the 555 is triggered when it falls below 2 V**
- **the 555 output is either 6 V (logic 1) or 0 V (logic 0)**
- **at a light level of 100 lux the resistance of the LDR is 10 kΩ.**

A suggested design for the circuit to meet the specification is shown opposite:

5. Evaluate the design using relevant calculations to determine if it meets the specification. Describe any modifications necessary.

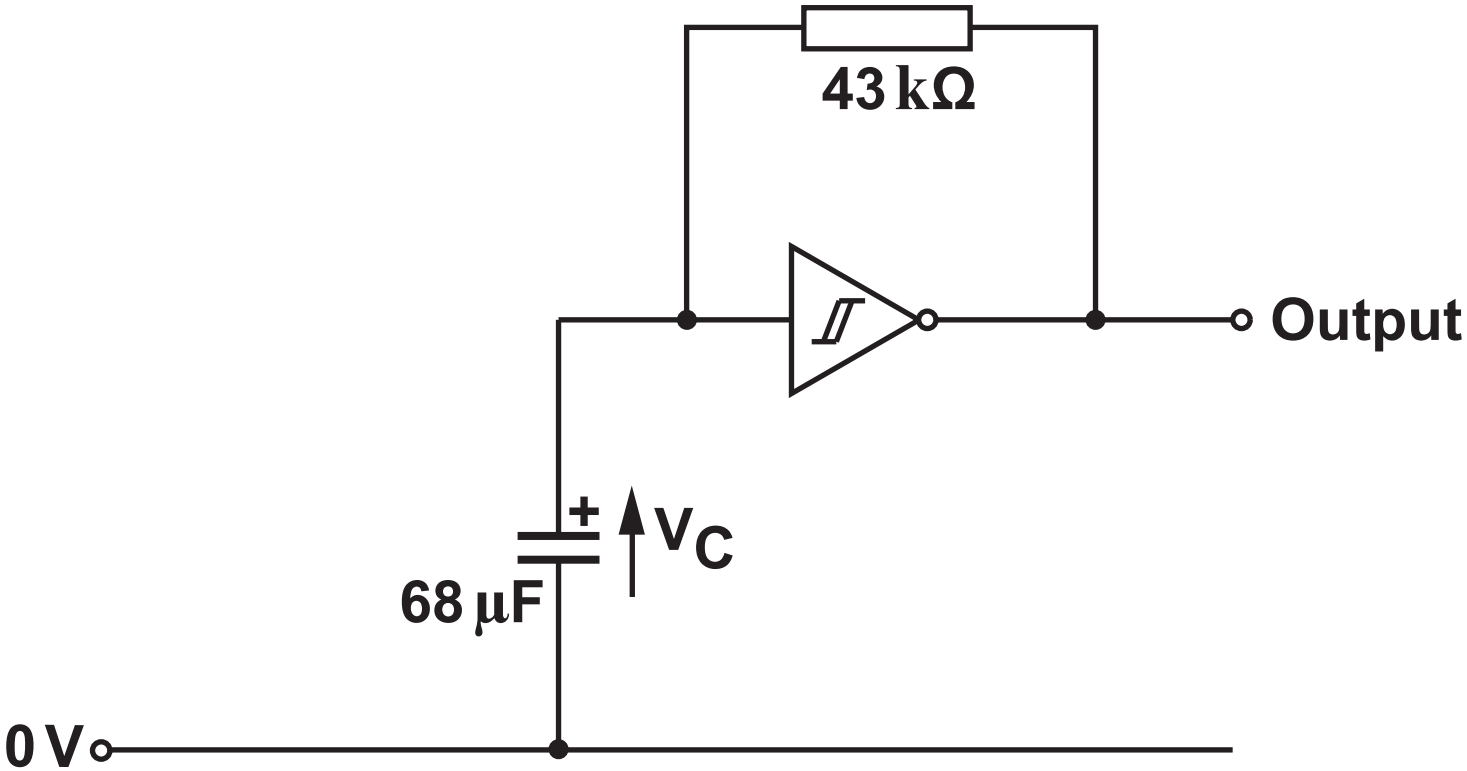
[6 marks QER]


+12 V
43 kΩ
+
68 µF
0 V

6 (a) **The circuit diagram opposite shows an RC network, connected to a 12 V supply.**

Calculate the time taken for the capacitor to charge from 0 V to 6 V when the switch is closed.

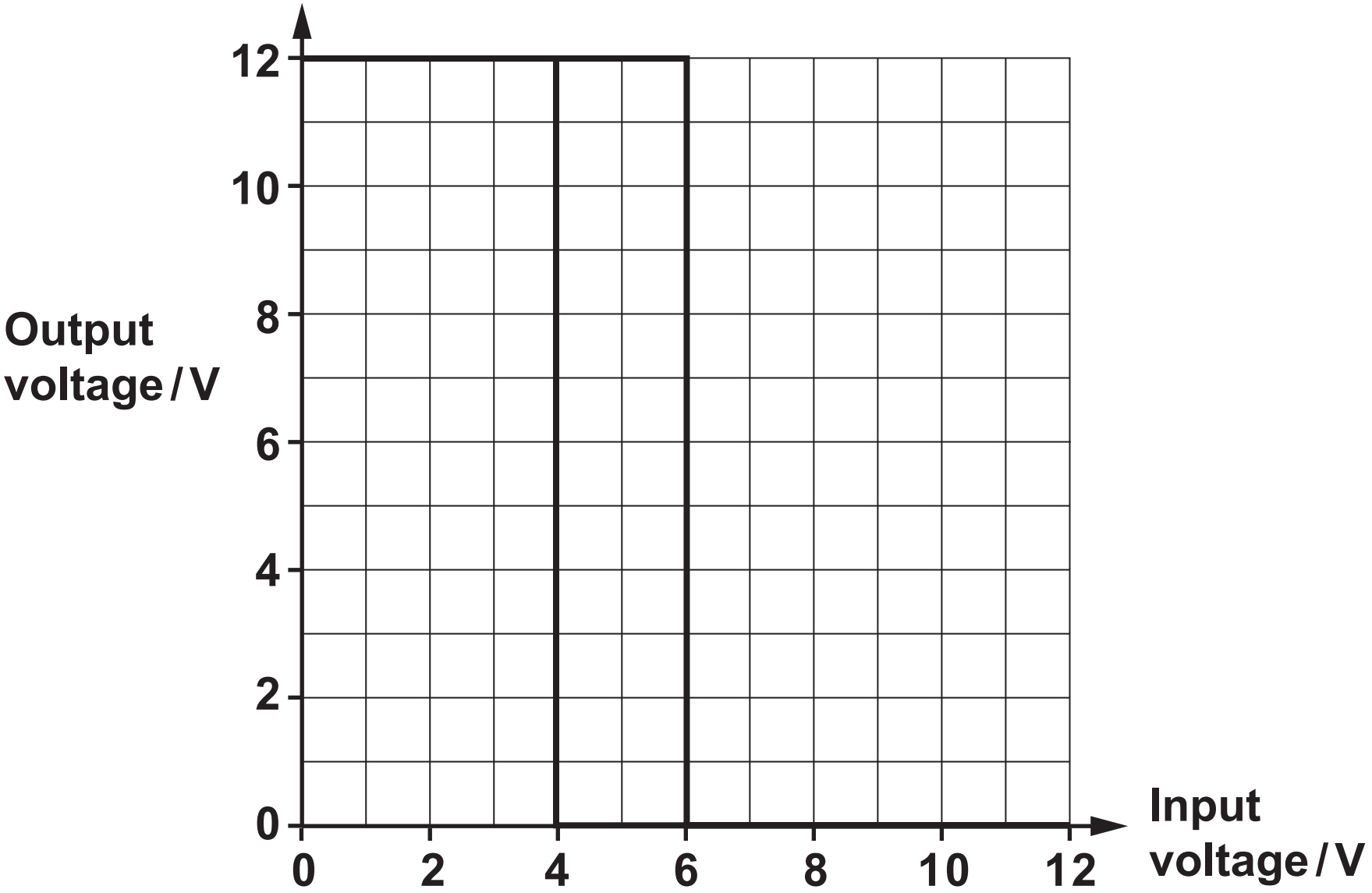
[2 marks]


43 kΩ
Output
±
V_C
68 µF
0 V

6 (b) **The same resistor and capacitor are used in an astable, based on a Schmitt inverter.**

The circuit is shown opposite:

(i) **Calculate the frequency and time period for this astable. [3 marks]**

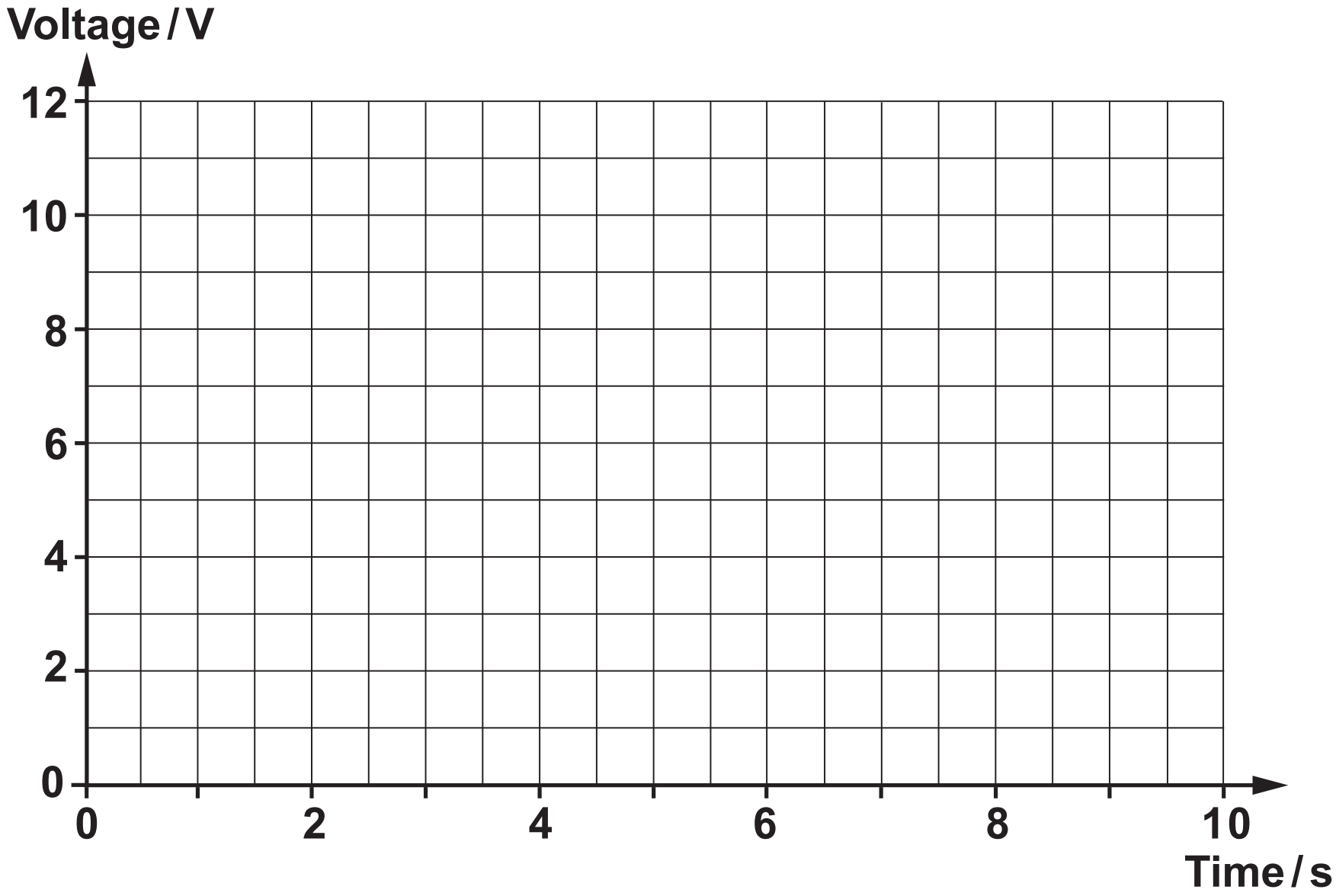

Output voltage / V
12
10
8
6
4
2
0
0
2
4
6
8
10
12
Input voltage / V

6 (b) (ii)

The characteristic of the Schmitt inverter is shown in the graph opposite.

I. What is the voltage V_C across the capacitor when the output voltage changes from 12 V to 0 V?

[1 mark]

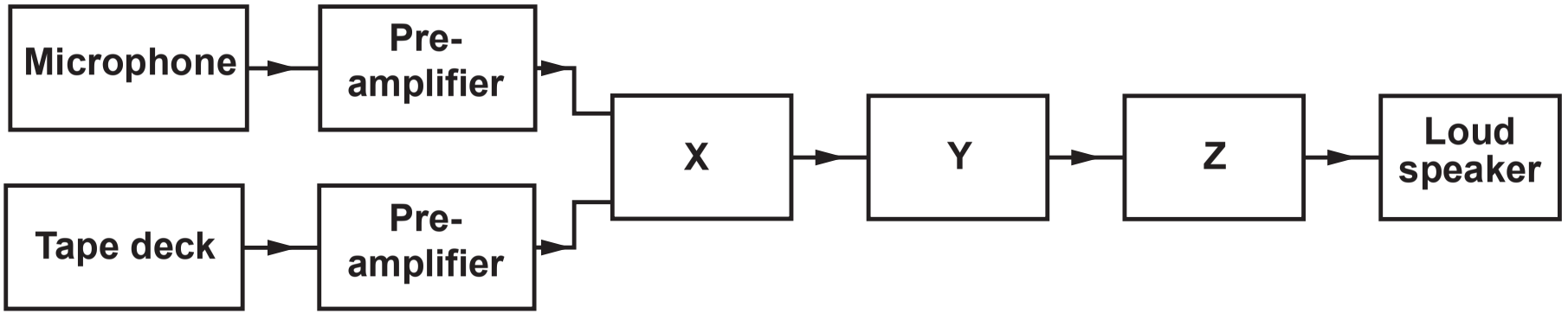

Voltage / V
12
10
8
6
4
2
0
0
2
4
6
8
10
Time / s

6 (b) (ii)

II. Complete the graph opposite to show the behaviour of the output of the astable over a period of 10 s after it has been running for some time. [3 marks]


Schmitt
astable
Output

6 (c) Design a sub-system using D-type flip-flops to divide the pulse frequency generated by the astable by four. (See diagram opposite). [5 marks]


Microphone
Pre-amplifier
Tape deck
Pre-amplifier
X
Y
Z
Loud speaker

7 (a) Identify blocks X, Y and Z for the following PA system opposite. [3 marks]

X = _____

Y = _____

Z = _____

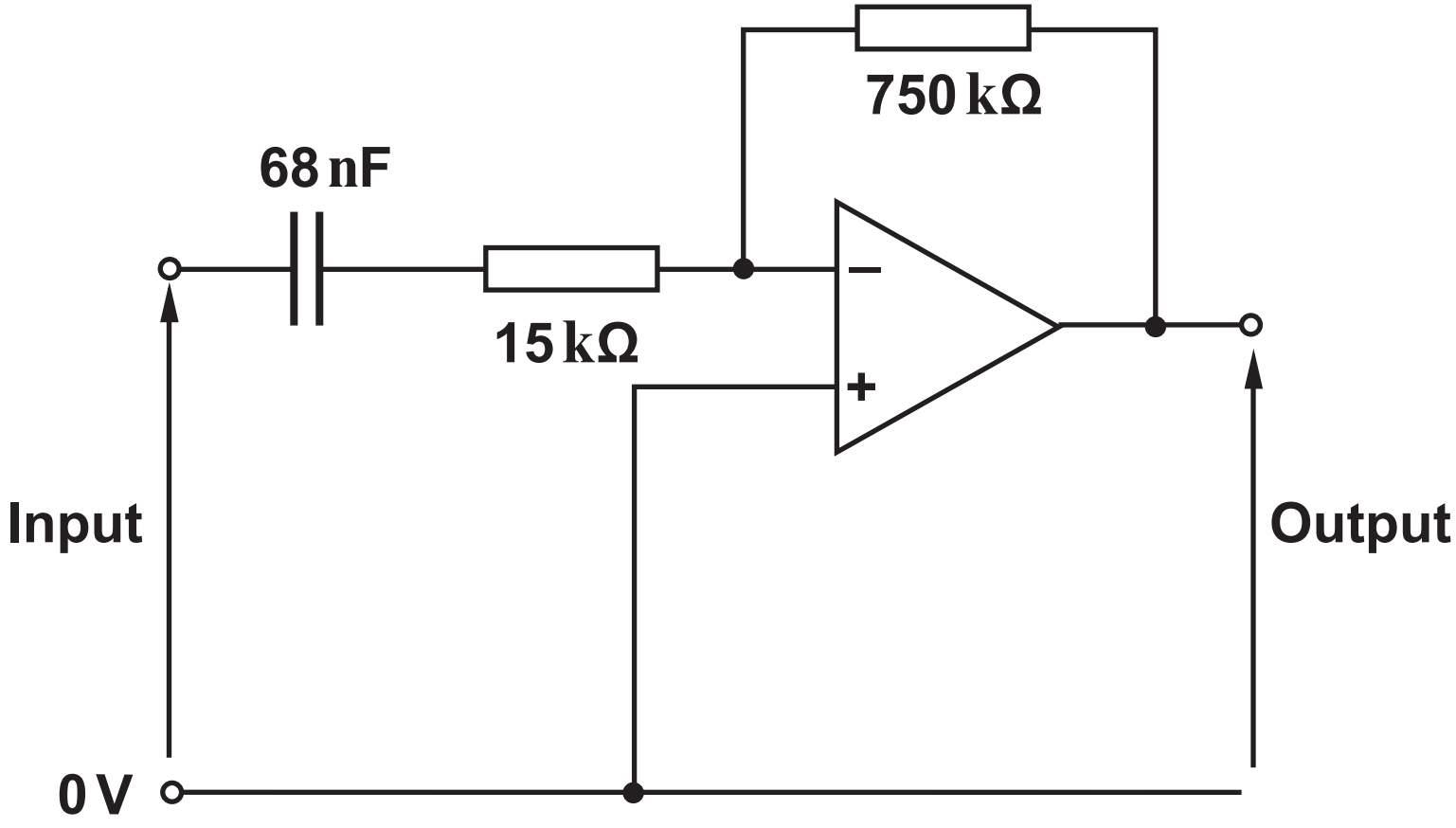
(b) What is the function of decoupling capacitors in a PA system? [1 mark]

_____

_____

_____

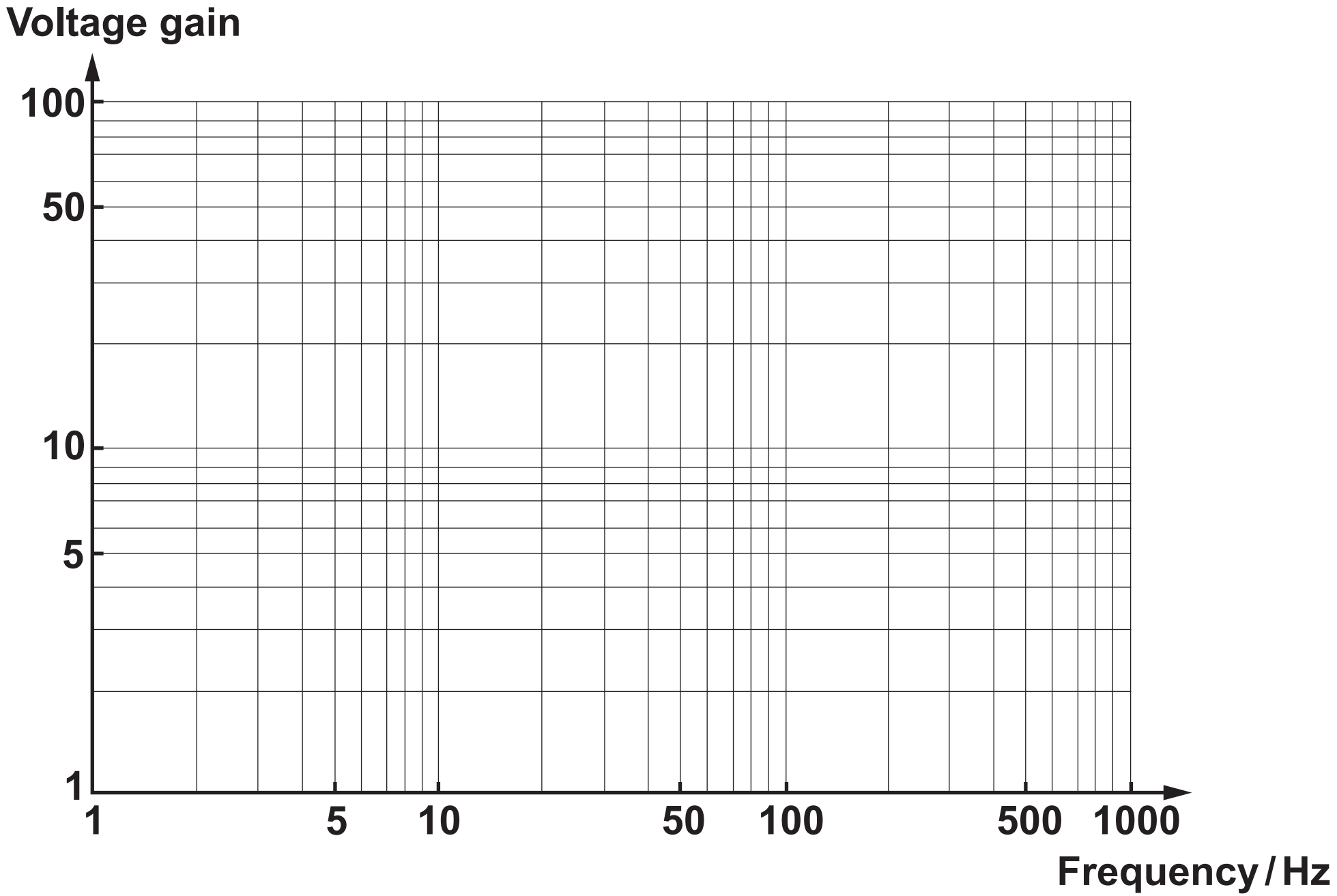
_____


750 kΩ
68 nF
15 kΩ
−
+
Input
Output
0 V

7 (c) The diagram opposite shows the circuit for an active filter.

(i) Give an advantage of an active filter over a passive filter. [1 mark]

(ii) Calculate the voltage gain and break frequency for this filter. [5 marks]


Voltage gain
100
50
10
5
1
1
5
10
50
100
500
1000
Frequency / Hz

7 (c) (iii) Use the axes to draw a graph opposite showing the frequency response of the filter. [5 marks]

(iv) To test the performance of the filter, two sinusoidal signals are applied to the input in turn.

The first has an amplitude of 75 mV and a frequency of 300 Hz.

The second has an amplitude of 75 mV and a frequency of 100 Hz.
What is the expected frequency and amplitude for each output signal?

Show any relevant calculations. [4 marks]

First signal:

_____

_____

_____

_____

Amplitude = _____

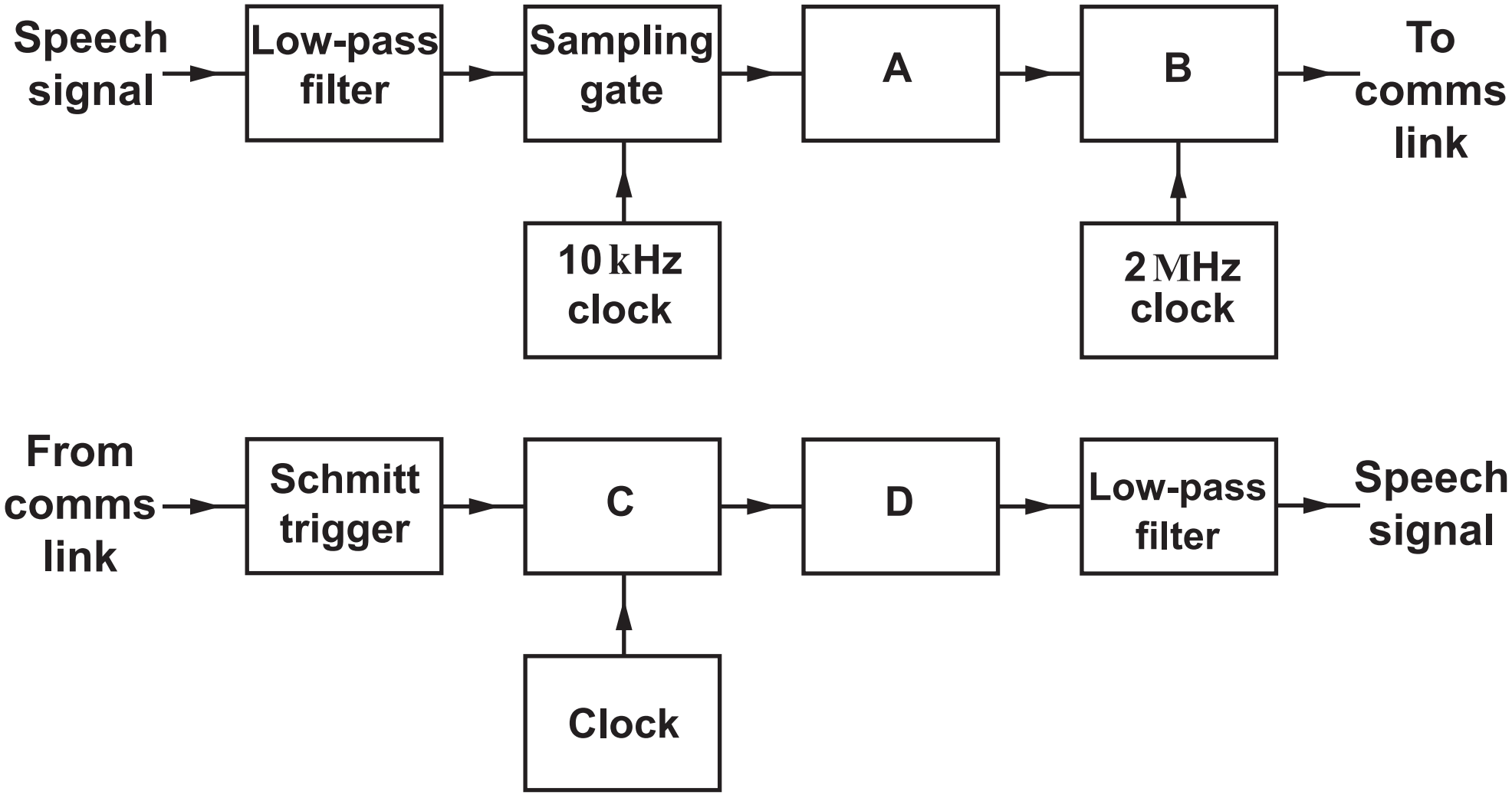
Frequency = _____

7 (c) (iv)

Second signal:

Amplitude = _____

Frequency = _____


Speech signal
Low-pass filter
Sampling gate
A
B
To comms link
10 kHz clock
2 MHz clock
From comms link
Schmitt trigger
C
D
Low-pass filter
Speech signal
Clock

8. The diagram opposite shows a digital communication system which uses pulse code modulation (PCM). It converts analogue speech signals into a stream of 10-bit digital signals. The digital stream is then transmitted down a communications link. At the receiver the digital stream is converted back into analogue signals.

(a) Identify the blocks labelled A to D. [4 marks]

A _____

B _____

C _____

D _____

8 (b) What is the maximum frequency of audio signal that this system can reproduce successfully?

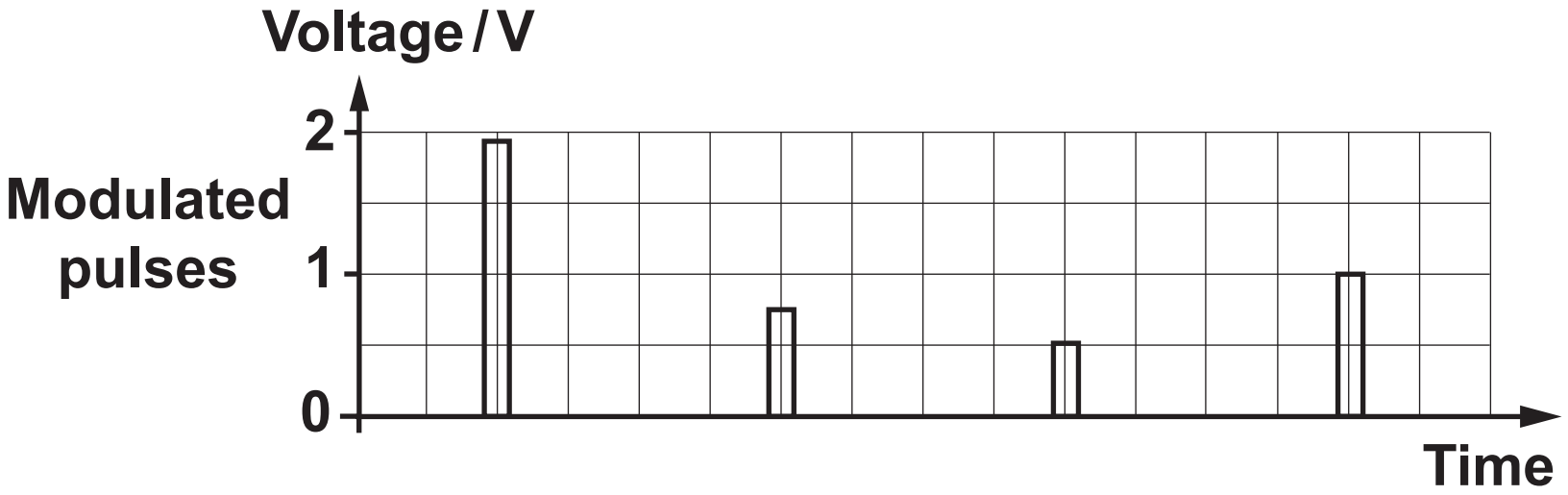
Explain how you obtain this answer. [2 marks]

(c) What is the function of each of the following blocks in the receiver?

(i) Schmitt trigger [1 mark]

8 (c) (ii)

low-pass filter [1 mark]


Voltage / V
2
1
0
Modulated pulses
Time

8 (d) The graph opposite shows a series of modulated pulses generated within the PCM system.

(i) What is the name for the type of modulation used here? [1 mark]

_____

_____

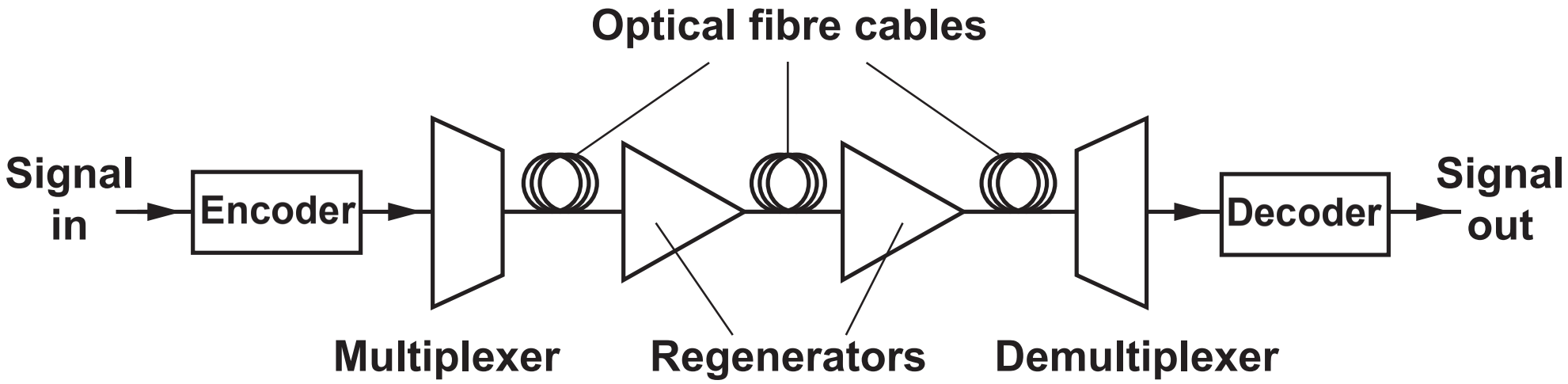
(ii) ON THE BLOCK DIAGRAM OF THE PCM SYSTEM OPPOSITE PAGE 34, add an arrow, labelled 'X', to show where this signal is found in the system. [1 mark]

8 (e) (i)

Distinguish between frequency division multiplexing (FDM) and time division multiplexing (TDM). [2 marks]

8 (e) (ii)

Using the information in the block diagram, opposite page 34. How many PCM channels identical to that can be combined into the TDM communications link? [4 marks]


Optical fibre cables
Signal in
Encoder
Multiplexer
Regenerators
Demultiplexer
Decoder
Signal out

9. The diagram opposite shows the structure of an optical fibre communications system.

(a) Dispersion and attenuation of light travelling down an optical fibre limit the length of cable that can be used between regenerators.

(i) Identify ONE cause of attenuation in an optical fibre cable. [1 mark]

_____

_____

_____

_____

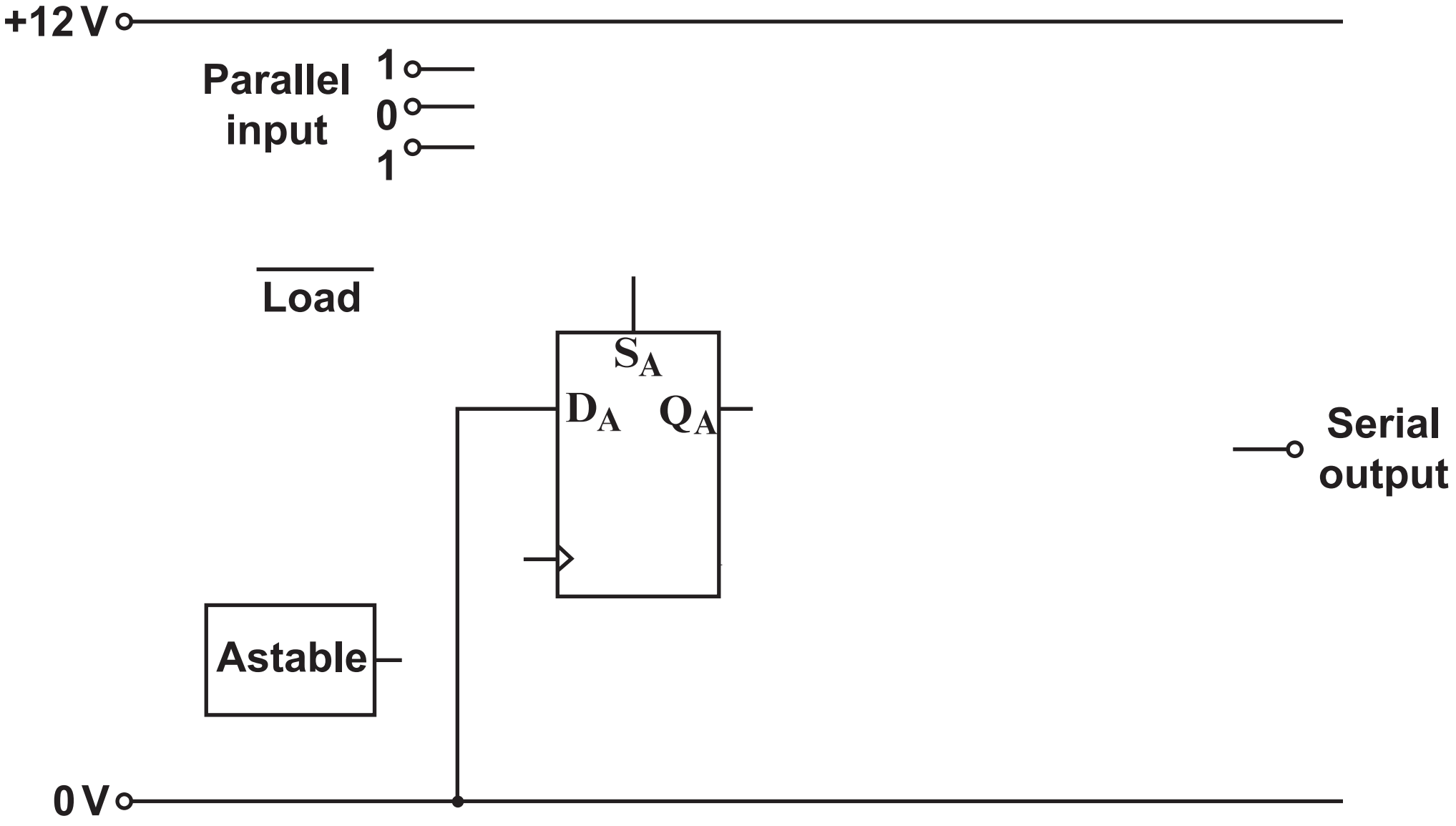
9 (a) (ii)

Dispersion causes a sharp pulse of light to spread out as it passes down the fibre.

Why does this happen? [1 mark]

9 (b) The regenerators are connected by an optical fibre cable 40 km long.
At the input, the signal has an optical power of 100 μW.
At the output of this cable, this has fallen to 5 μW.

Calculate the power loss, in dB / km, for this cable.
[3 marks]

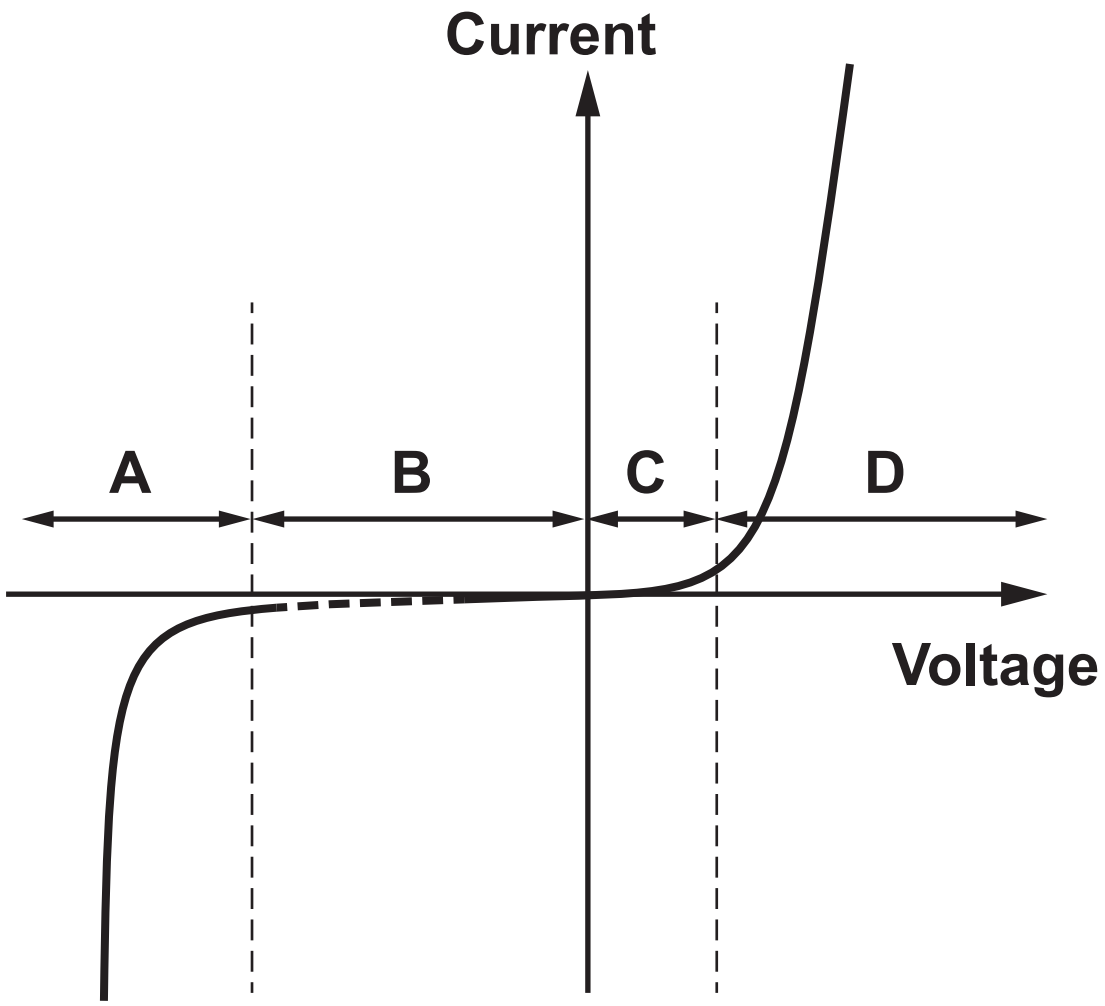

+12 V
Parallel input
1
0
1
Load
S_A
D_A
Q_A
Serial output
Astable
0 V

9 (c) **The encoder incorporates a parallel-in-series-out (PISO) register.**
A simplified PISO circuit is required to investigate the principles involved.

Design a suitable sub-system that:

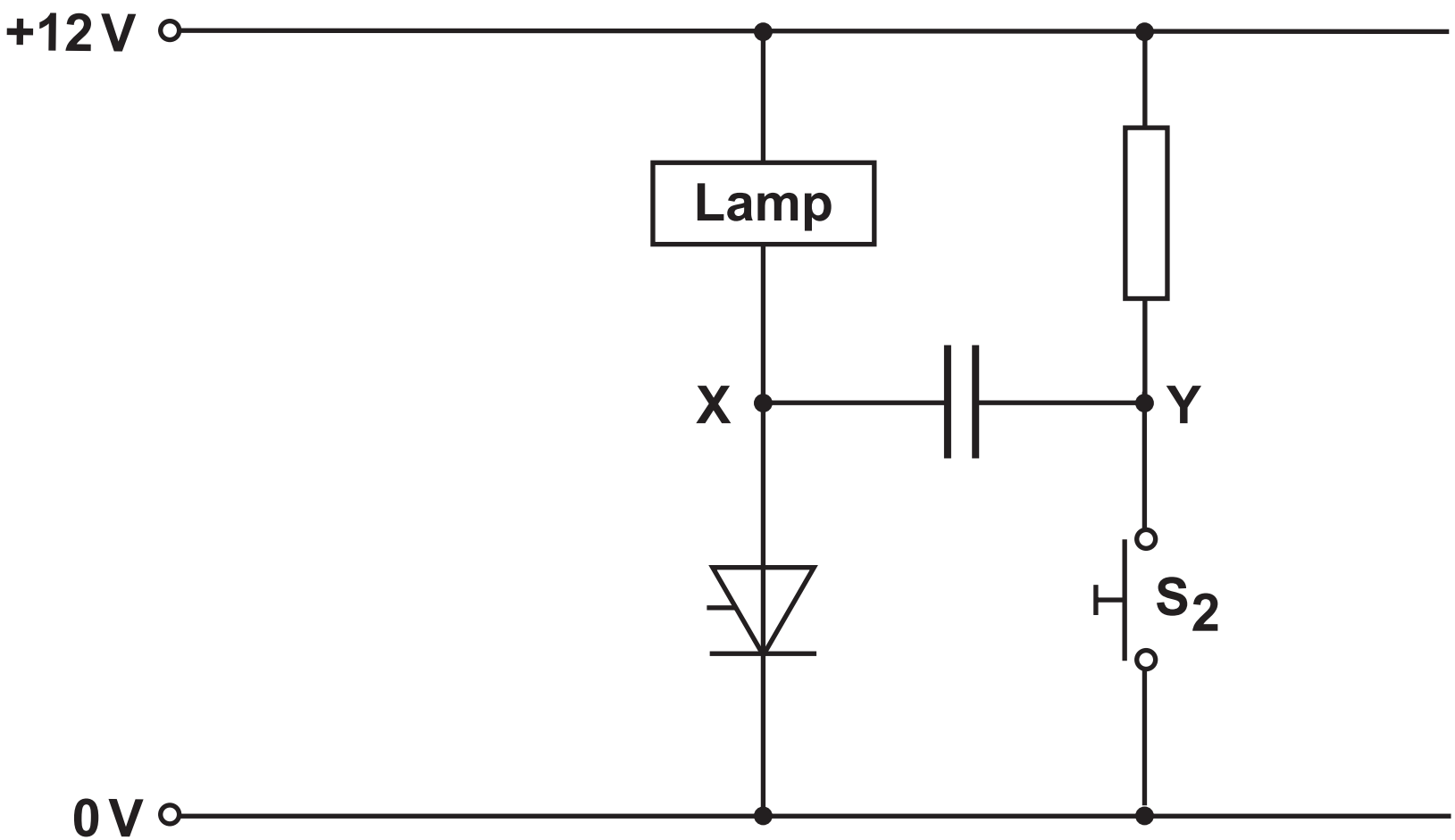
- **converts the input from parallel to serial format**
- **uses D-type flip-flops**
- **uses a switch unit to control the load input**
- **loads a 3-bit binary number '101'**
- **outputs this number as a serial stream of three single bits.**

The first D-type flip-flop is shown in the incomplete circuit diagram opposite. [6 marks]


Current
A
B
C
D
Voltage

9 (d) **The decoder uses a photodiode to convert the light pulses back into electrical pulses.**
Like all semiconductor diodes, this relies on the electrical properties of a p-n junction.
The diagram opposite shows the I-V characteristic of a p-n junction.

In which region of the graph, A, B, C or D, is the photodiode set up to operate? [1 mark]


+12 V
Lamp
X
Y
S2
0 V

10 (a) The diagram opposite shows part of a DC thyristor switching circuit, controlling a lamp.

(i) COMPLETE THE CIRCUIT by adding a switch, labelled S_1, and another component connected so that the lamp lights when switch S_1 is closed. [2 marks]

(ii) When the lamp is off and S_2 is open, what are the voltages at X and Y? [2 marks]

Voltage at X = _____

Voltage at Y = _____

(iii) When the lamp is lit and S_2 is open, what are the voltages at X and Y? [2 marks]

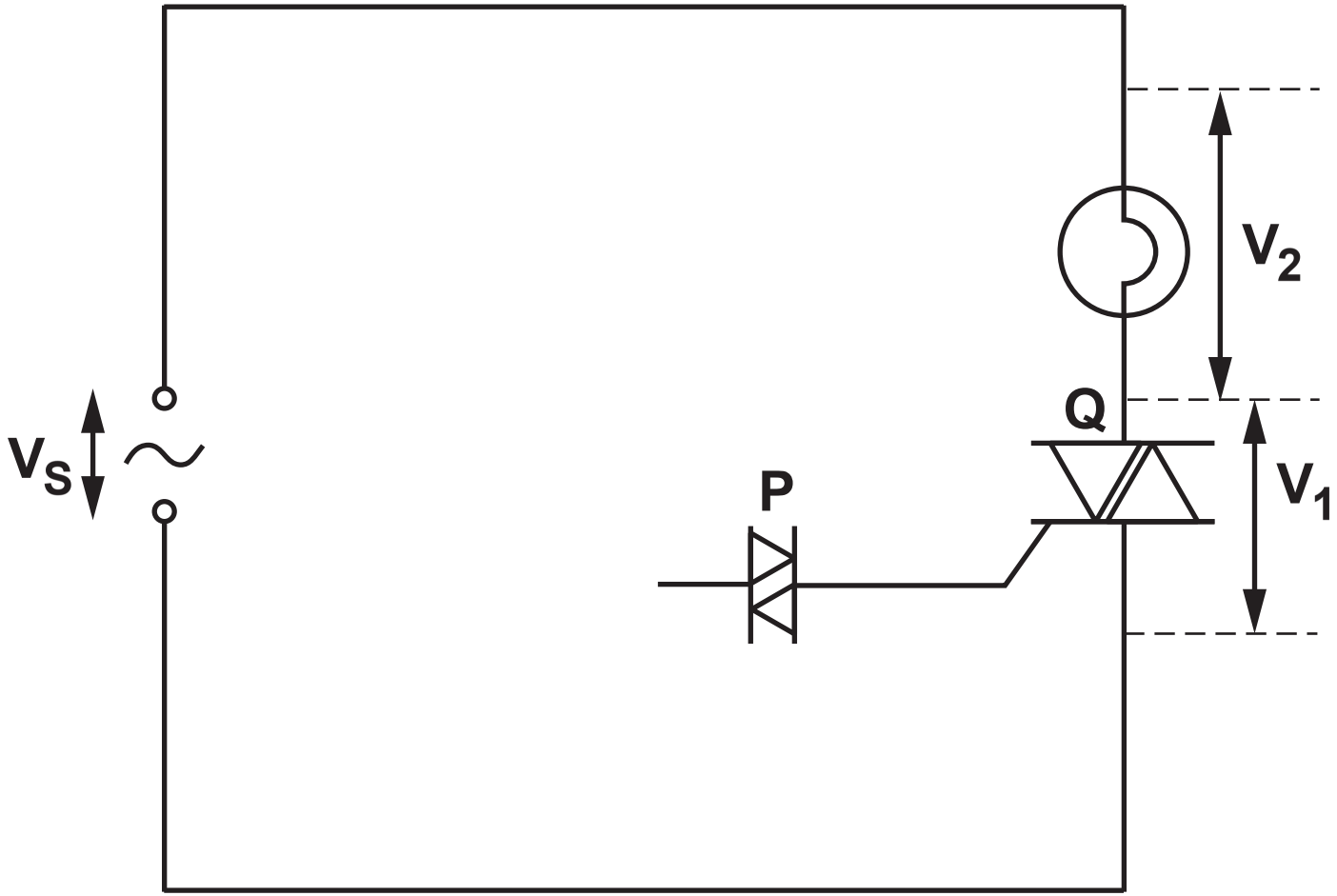
Voltage at X = _____

Voltage at Y = _____

10 (a) (iv)

When the lamp is lit, pressing switch S_2 for a moment turns it off.

Explain how this works. [2 marks]


V_S
P
Q
V_2
V_1

10 (b)

The diagram opposite shows part of a circuit for a lamp powered from an AC supply.

(i) COMPLETE THE DIAGRAM by adding TWO components to allow the brightness of the lamp to be varied using phase control. [3 marks]

(ii) State the name of:

component P _____

component Q _____

[2 marks]

10 (b) (iii)

The phase shift is set to zero. The upper graph opposite shows voltage V_1. The AC supply V_S is shown as a dashed line.

I. Use the lower axes to sketch the voltage V_2, across the lamp. [2 marks]

II. Add an arrow, labelled X, to show a time when the lamp is at its brightest. [1 mark]

END OF PAPER

Question number	Additional page, if required. Write the question numbers in the left-hand margin.

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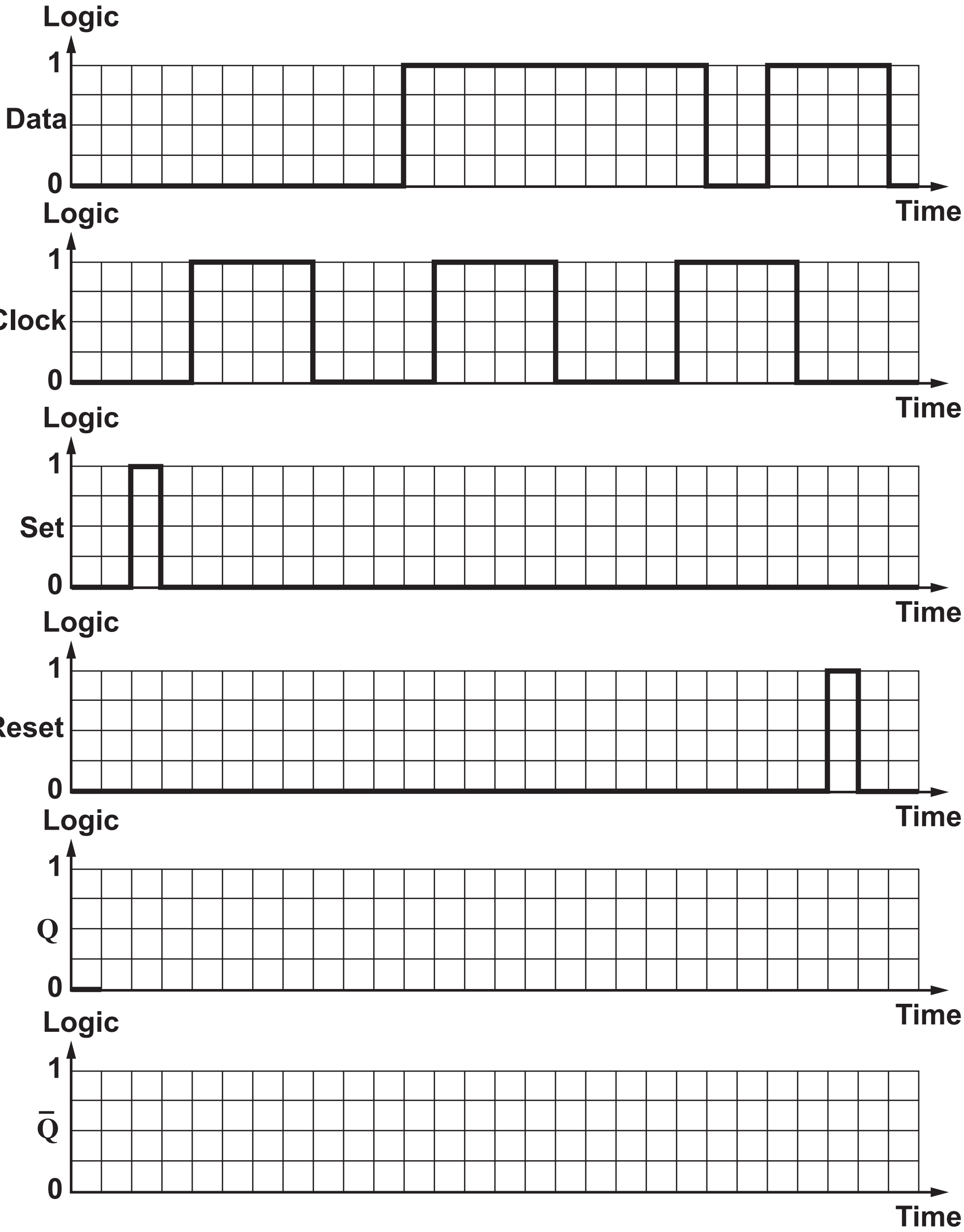
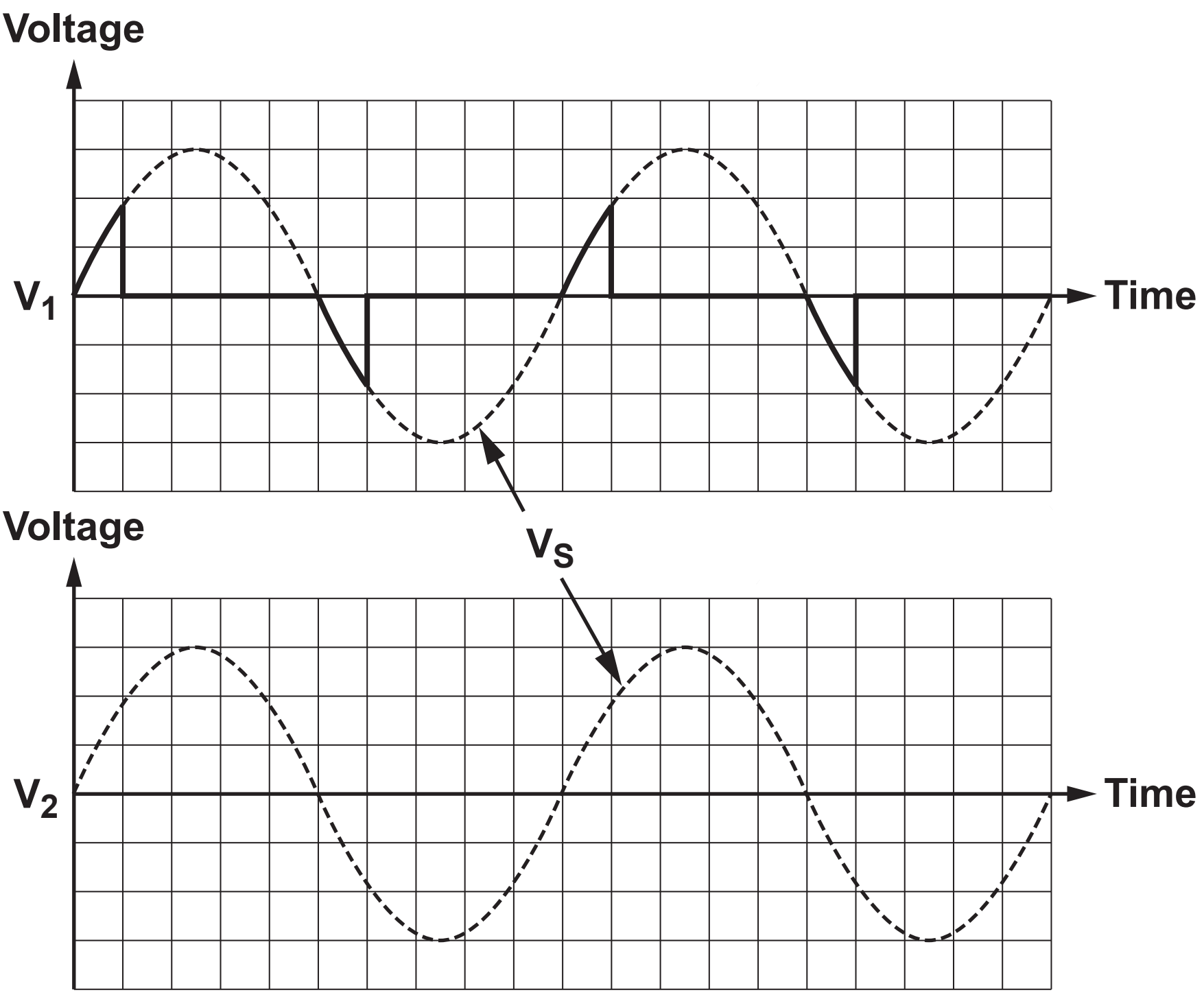

Logic
1
Data
0
Time
Logic
1
Clock
0
Logic
Time
1
Set
0
Logic
Time
Logic
1
Reset
0
Logic
Time
1
Q
0
Logic
Time
1
$\bar{Q}$
0
Time

```
100   begin   _____   _____   ; make sure all outputs are logic 0

101           _____   _____   ; is the switch pressed?

102           _____   begin   ; if it is not pressed repeat the check

103           bsf     _____   ; if it is pressed,  light the LED

104           call    onesec  ; delay

105           _____   _____   ;

106           _____   _____   ;

107           _____   _____   ; go back and start again
```


Voltage
V1
Time
Voltage
VS
V2
Time