| Surname | Centre Number | Candidate Number |
|---|---|---|
| First name(s) | | 2 |

# GCE A LEVEL

A490U20-1

S23-A490U20-1

**FRIDAY, 9 JUNE 2023 – AFTERNOON**

# ELECTRONICS – A level component 2

## Application of Electronics

2 hours 45 minutes

| For Examiner's use only | | |
|---|---|---|
| **Question** | **Maximum Mark** | **Mark Awarded** |
| **1.** | **10** | |
| **2.** | **18** | |
| **3.** | **13** | |
| **4.** | **16** | |
| **5.** | **6** | |
| **6.** | **14** | |
| **7.** | **19** | |
| **8.** | **16** | |
| **9.** | **12** | |
| **10.** | **16** | |
| **Total** | **140** | |

A490U201
01

### ADDITIONAL MATERIALS

You will require a calculator and a **Data Booklet**.

### INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen. Do not use gel pen or correction fluid.

You may use a pencil for graphs and diagrams only.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet. If you run out of space, use the additional page(s) at the back of the booklet, taking care to number the question(s) correctly.

### INFORMATION FOR CANDIDATES

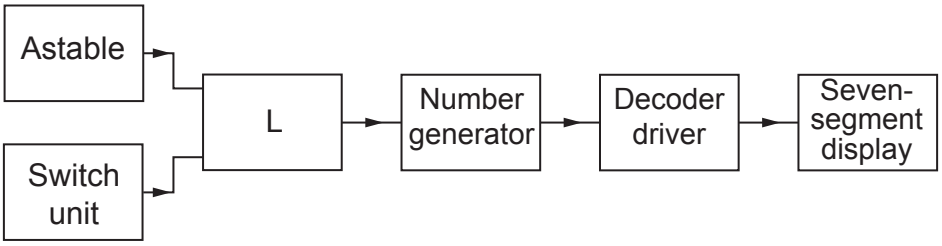
The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in question **5**.

Examiner only

Answer **all** questions.

**1.** The block diagram for an electronic dice is shown below:




When the switch is closed, the switch unit outputs a logic 0 signal and the number generator then repeatedly runs quickly through the number sequence from '1' to '6'.

When the switch is then opened, the sequence stops and a fixed number is displayed.

(a) What type of logic gate must be used in block L in this system? [1]

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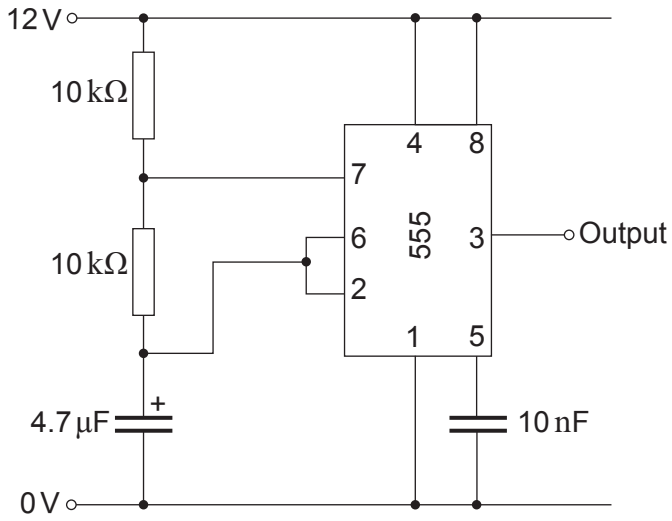
(b) The astable uses a 555 timer IC. The circuit is shown below.




Calculate:

(i) the frequency of the astable; [2]

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Examiner only

(ii) the mark/space ratio of the pulse train produced. [2]

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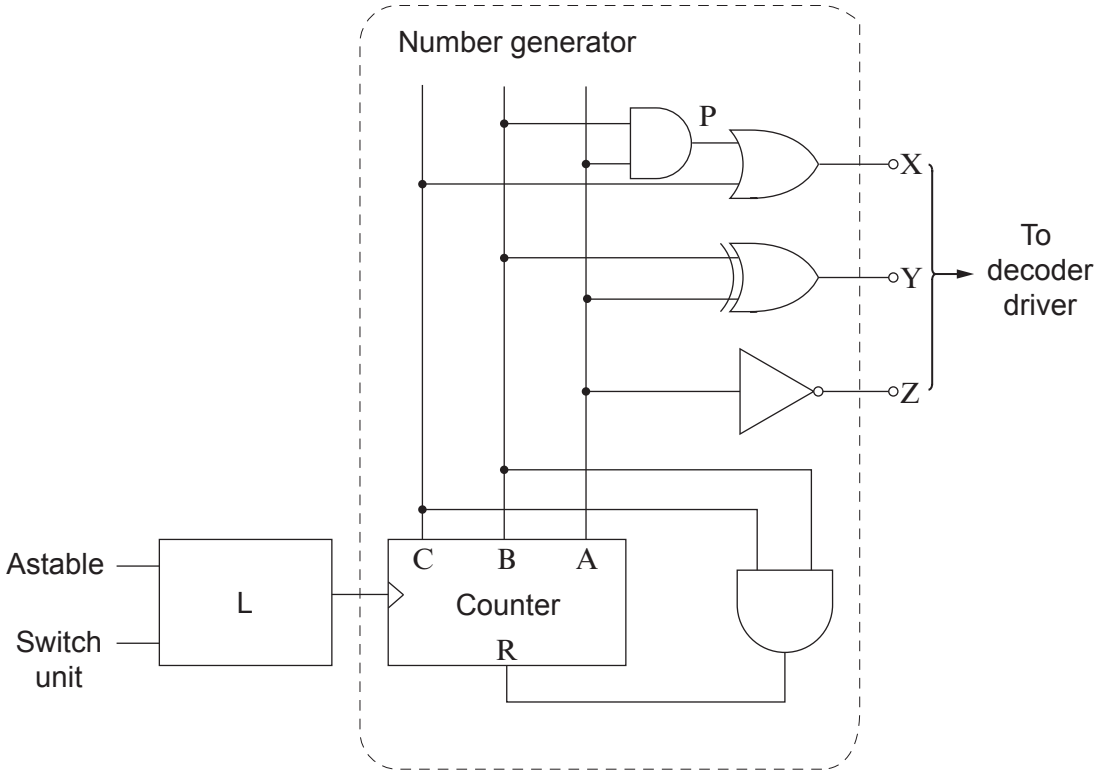
(c) A student designs the following counter and combinational logic system to generate the number sequence.




Complete the truth table for the number generator. [5]

| C | B | A | P | X | Y | Z |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | | |
| 0 | 0 | 1 | | | | |
| 0 | 1 | 0 | | | | |
| 0 | 1 | 1 | | | | |
| 1 | 0 | 0 | | | | |
| 1 | 0 | 1 | | | | |
| 1 | 1 | 0 | | | | |
| 1 | 1 | 1 | | | | |

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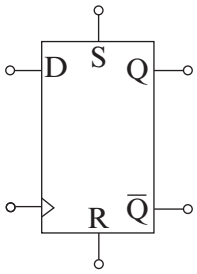
**2.** (a) The diagram shows the symbol for a D-type flip-flop including Set ($S$) and Reset ($R$) inputs.
It is rising-edge triggered and the set and reset inputs are both active-high.




The graphs show the signals applied to the inputs.
Complete the timing diagrams to show the resulting $Q$ and $\overline{Q}$ outputs.
The $Q$ output is initially at logic 0. [5]

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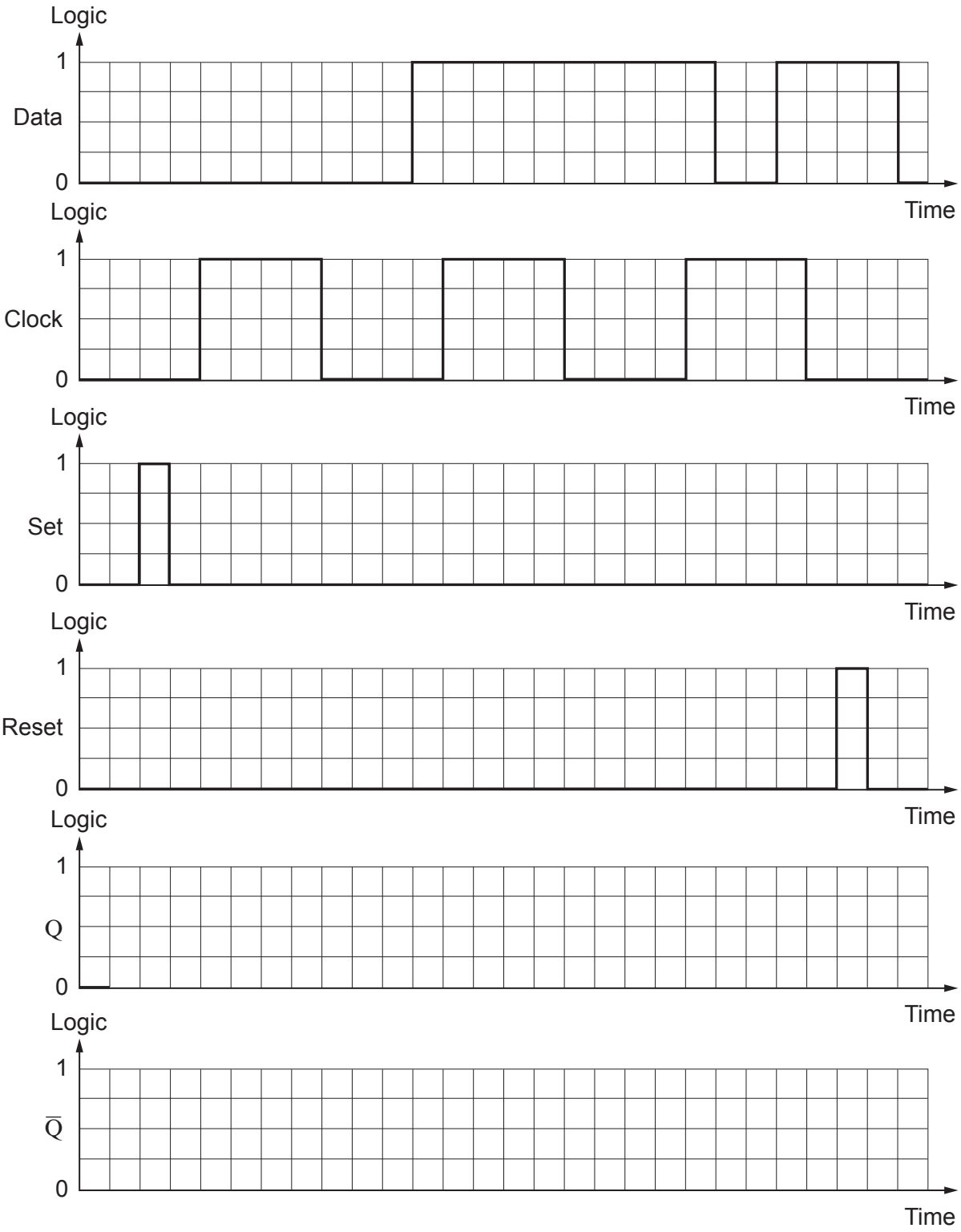


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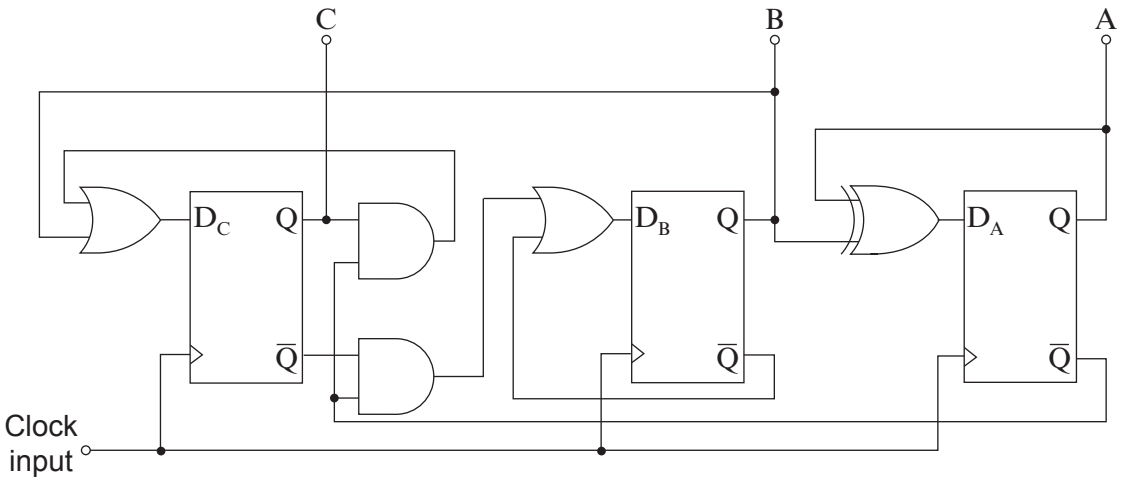
(b) Three D-type flip-flops are connected as a sequence generator.
(The set and reset inputs are not used and all are connected to 0 V.)




(i) Complete Boolean expressions linking the inputs $D_C$, $D_B$ and $D_A$ to outputs C, B and A. [5]

$D_C$ = .....

$D_B$ = .....

$D_A$ = .....

(ii) Complete the truth table for the sequence generator. [4]

| Current state | | | Next state | | |
|---|---|---|---|---|---|
| C | B | A | $D_C$ | $D_B$ | $D_A$ |
| 1 | 0 | 0 | | | |
| | | | | | |
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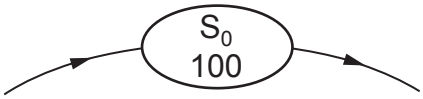
(iii) Use the truth table to determine the main sequence and unused states. Hence, draw the state diagram. [2]




(iv) It is important that a sequence generator is designed to avoid stuck states.

What are stuck states and why must a sequence generator avoid them? [2]

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**3.** A microcontroller is programmed to wait for a switch to be pressed and then light an LED for 3 s.

It uses a switch unit which outputs a logic 1 signal when the switch is pressed.

The switch unit is connected to Port A bit 7 of a PIC 16F88 microcontroller. All other bits of Port A are set as outputs.

(a) Complete the following instructions to set up Port A as described above. [3]

movlw b'.....'

..... .....

(b) An LED, connected to Port A bit 2, lights when it receives a logic 1 signal.
A delay subroutine, called onesec, is available. It creates a one second time delay.

Complete the following section of code that:
- waits for the switch to be pressed
- then lights the LED for three seconds
- then waits for the switch to be pressed again. [10]

```
100   begin   .....   .....   ; make sure all outputs are logic 0
101           .....   .....   ; is the switch pressed?
102           .....   begin   ; if it is not pressed repeat the check
103           bsf     .....   ; if it is pressed, light the LED
104           call    onesec  ; delay
105           .....   .....   ;
106           .....   .....   ;
107           .....   .....   ; go back and start again
```

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Examiner only

**4.** (a) Complete the diagram for a smoothed full-wave rectifier. [3]


(b) Power supplies often have good 'load regulation'. Explain what is meant by 'load regulation'. [2]

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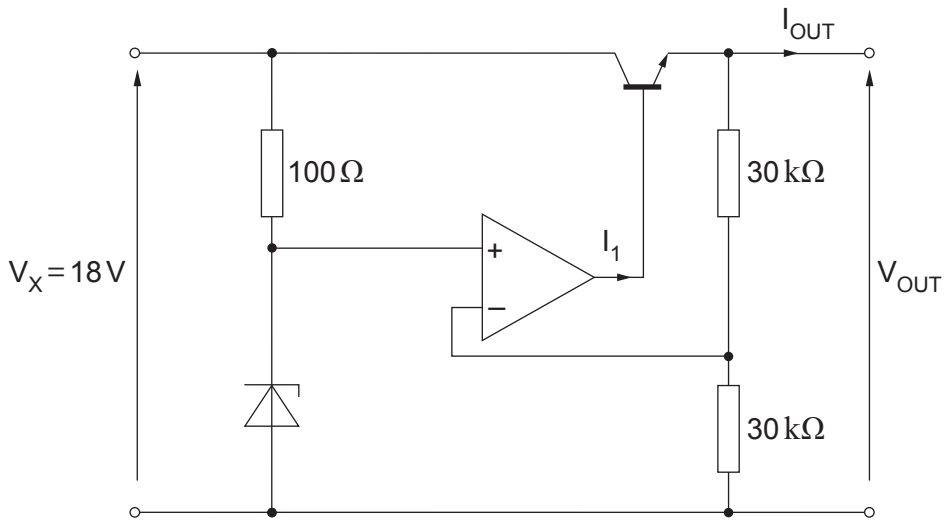
(c) The following circuit is added to the output of this full-wave rectifier.




(i) The output voltage $V_{OUT}$ = 15 V.
Circle a suitable value of zener voltage from the list and justify your answer with a calculation. [3]

Possible zener voltage values:

3 V  7.5 V  10 V  15 V  18 V

Justification:

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Examiner only

(ii) The transistor has a current gain, $h_{FE}$ of 40.
With a load connected the current $I_{OUT}$ = 320 mA.
The currents flowing into the inputs of the op-amp are negligibly small.
Calculate the current $I_1$ delivered by the op-amp. [2]

(iii) Calculate the power dissipated in the zener diode. [3]

(iv) Explain the role of the non-inverting amplifier in this power supply when the output voltage $V_{OUT}$ starts to decrease. [3]

Examiner only

**5.** A student photographer wants a system that lights an LED when the light level is so low that additional lighting from a flash is needed.

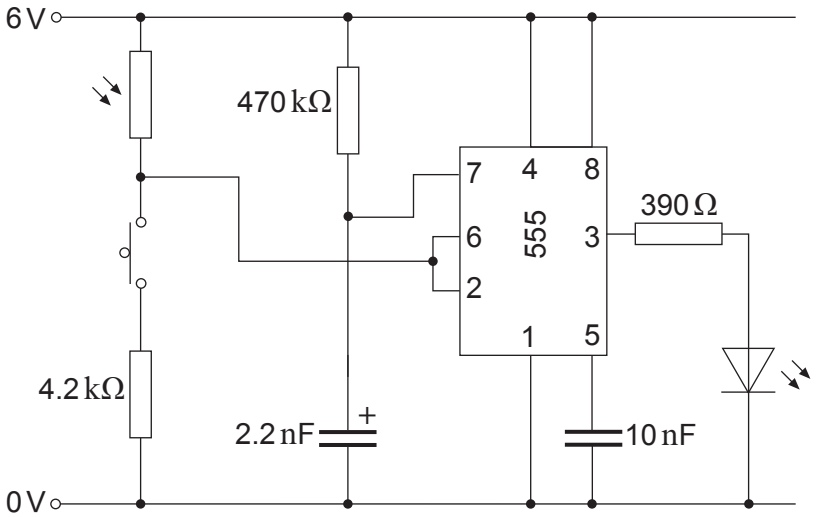
The specification for the system is as follows:

- it runs off a 6 V battery
- an LED lights for one second if the light level is too low
- the system is triggered by a push switch provided that the light level is below 100 lux.

The following information is used in designing the system:

- the LED passes a current of approximately 10 mA when lit and has a forward voltage drop of 2 V
- pin 2 of the 555 is triggered when it falls below 2 V
- the 555 output is either 6 V (logic 1) or 0 V (logic 0)
- at a light level of 100 lux the resistance of the LDR is 10 kΩ.

A suggested design for the circuit to meet the specification is shown below:




Evaluate the design using relevant calculations to determine if it meets the specification. Describe any modifications necessary. [6 QER]

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6



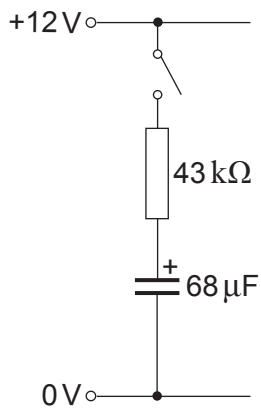




**Turn over.**

Examiner only

**6.** (a) The circuit diagram shows an RC network, connected to a 12 V supply.




Calculate the time taken for the capacitor to charge from 0 V to 6 V when the switch is closed. [2]

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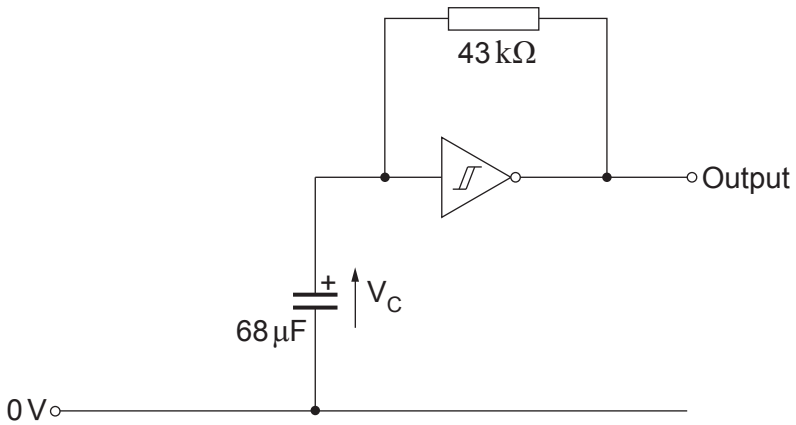
(b) The same resistor and capacitor are used in an astable, based on a Schmitt inverter. The circuit is shown below:




(i) Calculate the frequency and time period for this astable. [3]

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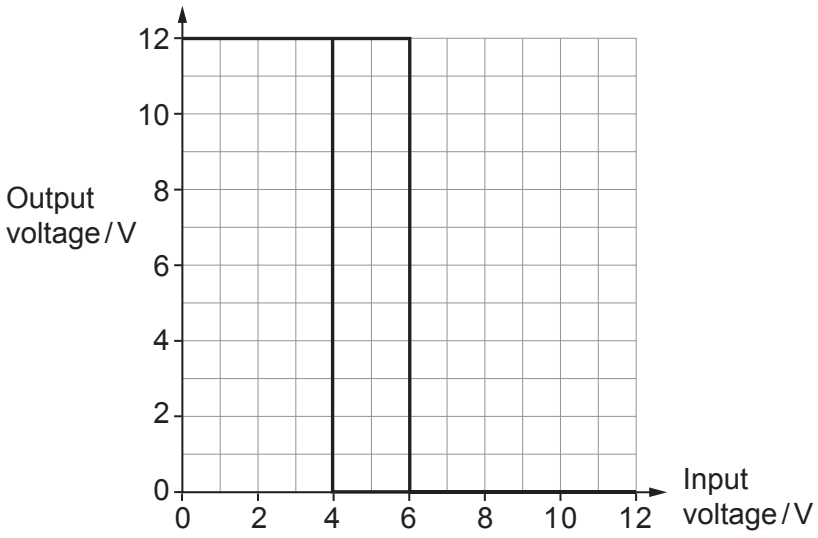
Examiner only

(ii) The characteristic of the Schmitt inverter is shown in the following graph.




I. What is the voltage $V_C$ across the capacitor when the output voltage changes from 12 V to 0 V? [1]

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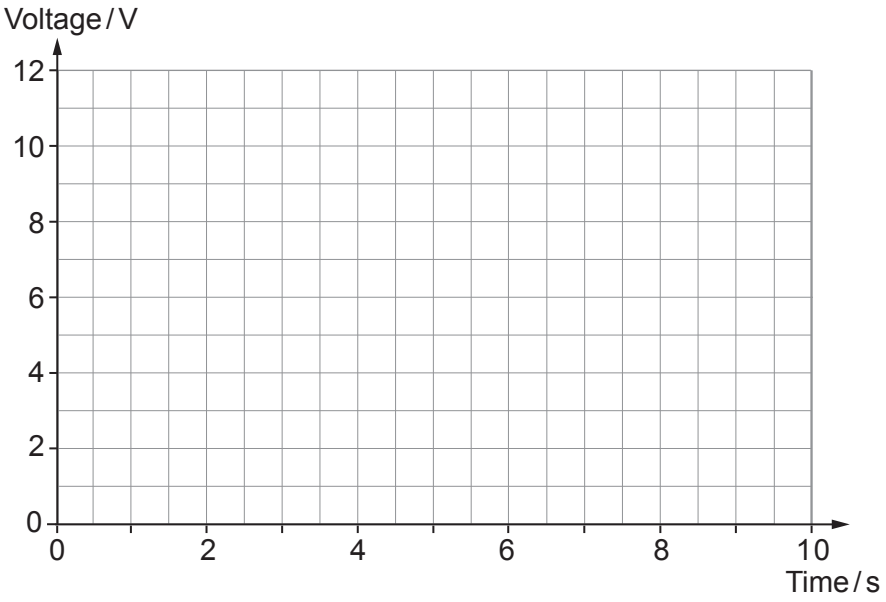
II. Complete the graph to show the behaviour of the output of the astable over a period of 10 s after it has been running for some time. [3]



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(c) Design a sub-system using D-type flip-flops to divide the pulse frequency generated by the astable by four. [5]


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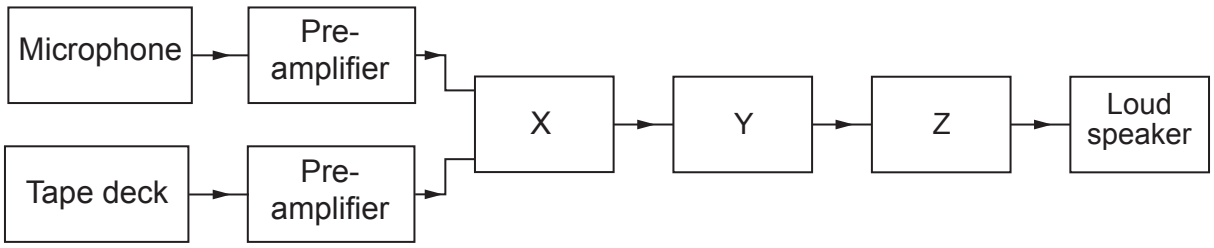
**7.** (a) Identify blocks X, Y and Z for the following PA system. [3]




X = .....

Y = .....

Z = .....

(b) What is the function of decoupling capacitors in a PA system? [1]

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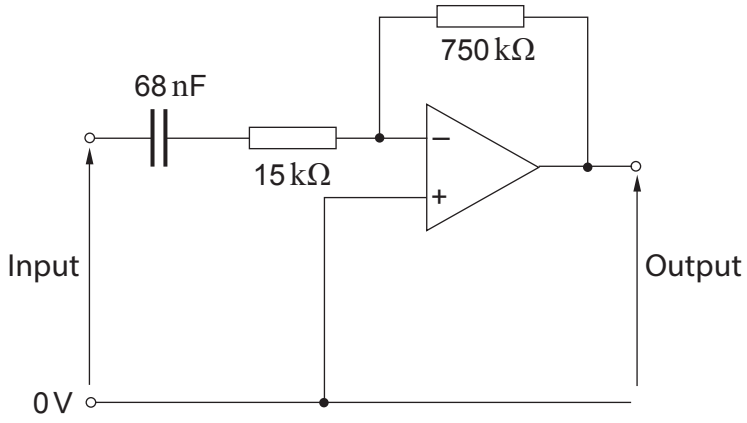
(c) The diagram shows the circuit for an active filter.




(i) Give an advantage of an active filter over a passive filter. [1]

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(ii) Calculate the voltage gain and break frequency for this filter. [5]

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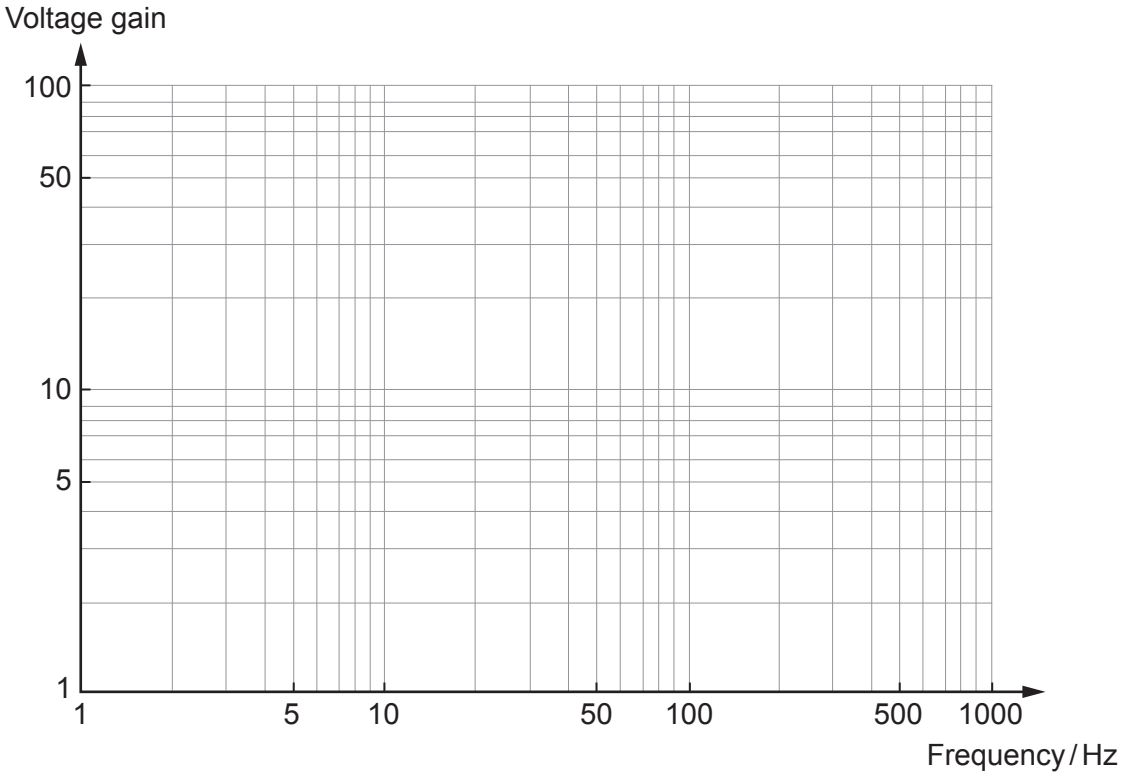
(iii) Use the axes to draw a graph showing the frequency response of the filter. [5]



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(iv) To test the performance of the filter, two sinusoidal signals are applied to the input in turn.
The first has an amplitude of 75 mV and a frequency of 300 Hz.
The second has an amplitude of 75 mV and a frequency of 100 Hz.
What is the expected frequency and amplitude for each output signal?
Show any relevant calculations. [4]

First signal:

.....

.....

Amplitude = ..... Frequency = .....

Second signal:

.....

.....

Amplitude = ..... Frequency = .....

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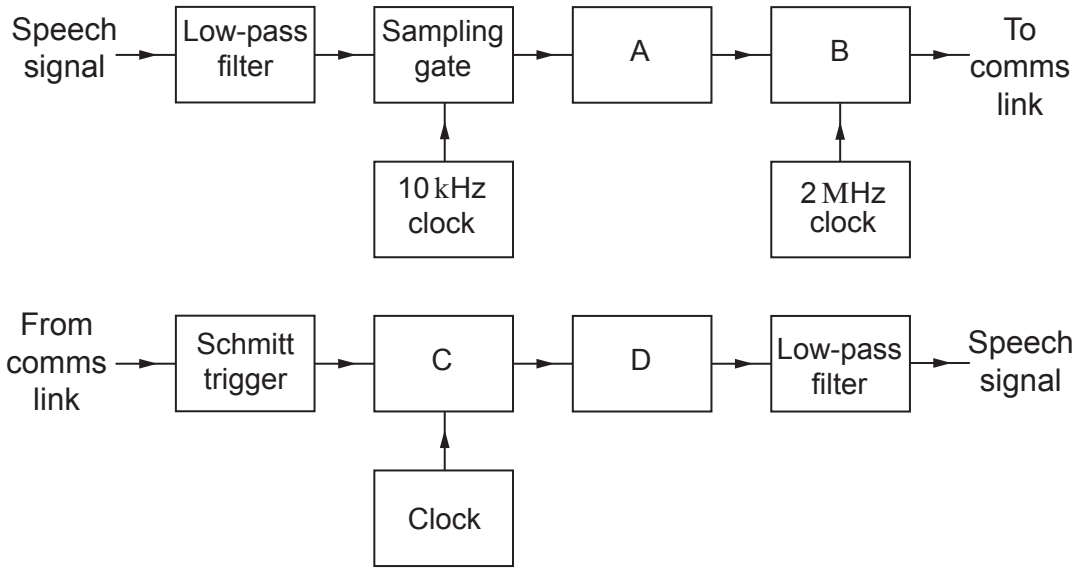
**8.** Here is a diagram for a digital communication system which uses pulse code modulation (PCM). It converts analogue speech signals into a stream of 10-bit digital signals. The digital stream is then transmitted down a communications link. At the receiver the digital stream is converted back into analogue signals.




(a) Identify the blocks labelled A to D. [4]

A .....

B .....

C .....

D .....

(b) What is the maximum frequency of audio signal that this system can reproduce successfully?
Explain how you obtain this answer. [2]

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(c) What is the function of each of the following blocks in the receiver?

(i) Schmitt trigger [1]

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(ii) low-pass filter [1]

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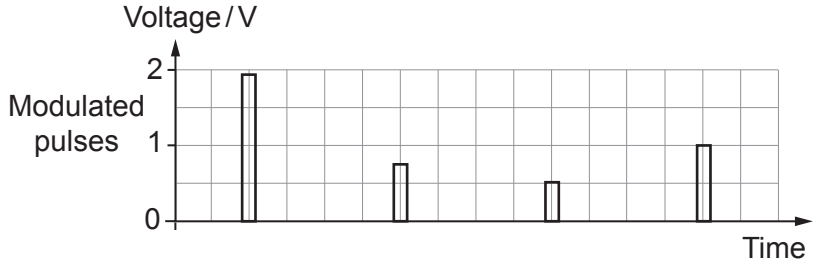
(d) The graph shows a series of modulated pulses generated within the PCM system.




(i) What is the name for the type of modulation used here? [1]

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(ii) **On the block diagram of the PCM system above**, add an arrow, labelled 'X', to show where this signal is found in the system. [1]

(e) (i) Distinguish between frequency division multiplexing (FDM) and time division multiplexing (TDM). [2]

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(ii) Using the information in the block diagram. How many PCM channels identical to that above can be combined into the TDM communications link? [4]

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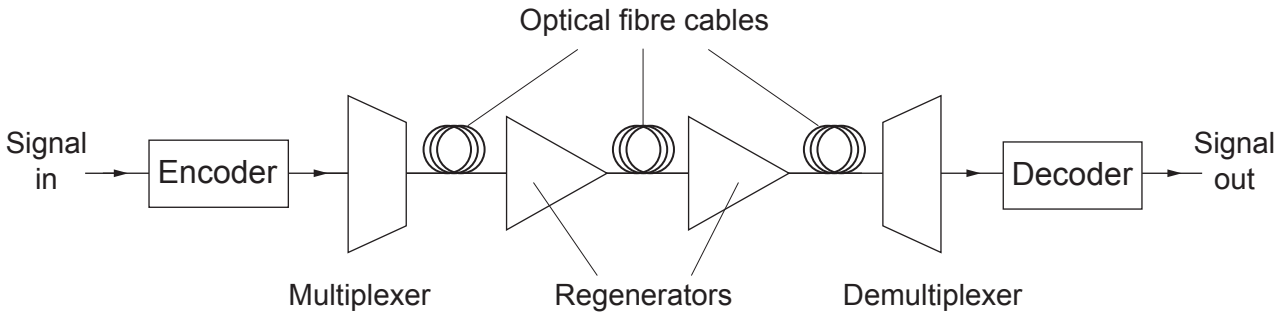
**9.** The diagram shows the structure of an optical fibre communications system.




(a) Dispersion and attenuation of light travelling down an optical fibre limit the length of cable that can be used between regenerators.

(i) Identify **one** cause of attenuation in an optical fibre cable. [1]

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(ii) Dispersion causes a sharp pulse of light to spread out as it passes down the fibre. Why does this happen? [1]

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(b) The regenerators are connected by an optical fibre cable 40 km long.
At the input, the signal has an optical power of 100 μW.
At the output of this cable, this has fallen to 5 μW.

Calculate the power loss, in dB / km, for this cable. [3]

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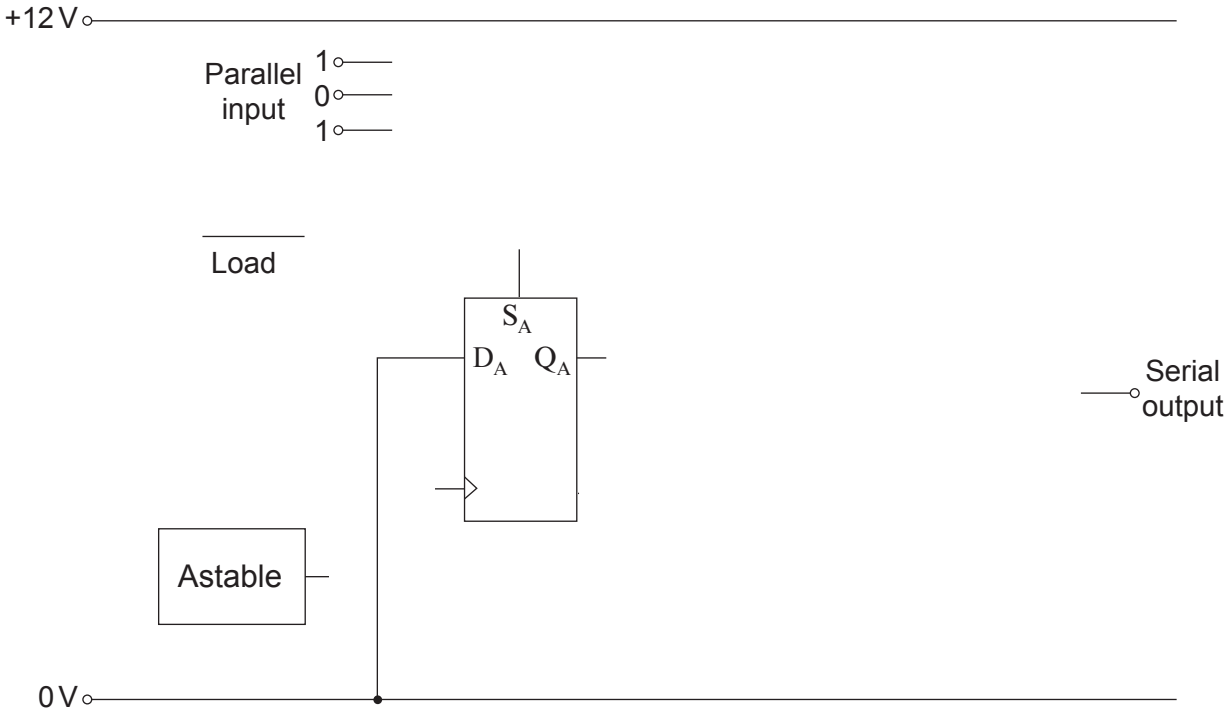
(c) The encoder incorporates a parallel-in-series-out (PISO) register.
A simplified PISO circuit is required to investigate the principles involved.

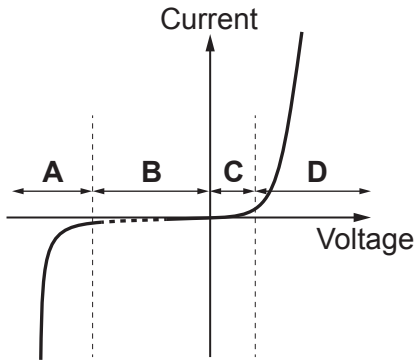
Design a suitable sub-system that:

- converts the input from parallel to serial format
- uses D-type flip-flops
- uses a switch unit to control the load input
- loads a 3-bit binary number '101'
- outputs this number as a serial stream of three single bits.

The first D-type flip-flop is shown in the incomplete circuit diagram. [6]




(d) The decoder uses a photodiode to convert the light pulses back into electrical pulses.
Like all semiconductor diodes, this relies on the electrical properties of a p-n junction.
The diagram shows the I-V characteristic of a p-n junction.




In which region of the graph, **A**, **B**, **C** or **D**, is the photodiode set up to operate? [1]

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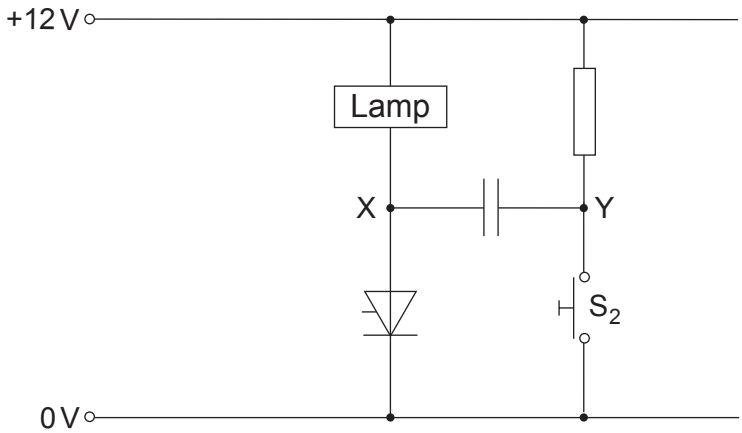
**10.** (a) The diagram shows part of a DC thyristor switching circuit, controlling a lamp.




(i) **Complete the circuit** by adding a switch, labelled $S_1$, and another component connected so that the lamp lights when switch $S_1$ is closed. [2]

(ii) When the lamp is off and $S_2$ is open, what are the voltages at X and Y? [2]

Voltage at X = ..... Voltage at Y = .....

(iii) When the lamp is lit and $S_2$ is open, what are the voltages at X and Y? [2]

Voltage at X = ..... Voltage at Y = .....

(iv) When the lamp is lit, pressing switch $S_2$ for a moment turns it off. Explain how this works. [2]

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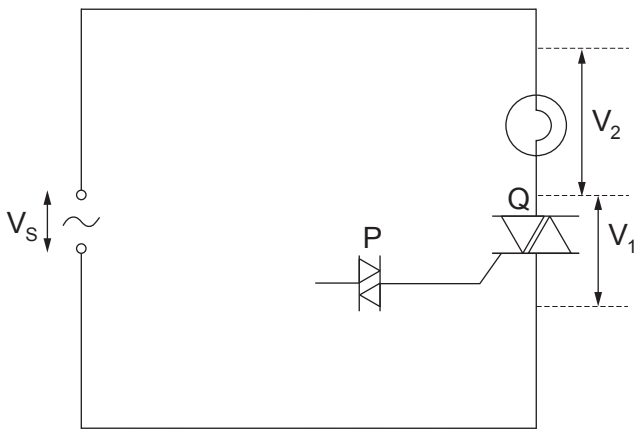
(b) The following diagram shows part of a circuit for a lamp powered from an AC supply.

(i) **Complete the diagram** by adding **two** components to allow the brightness of the lamp to be varied using phase control. [3]



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(ii) State the name of:

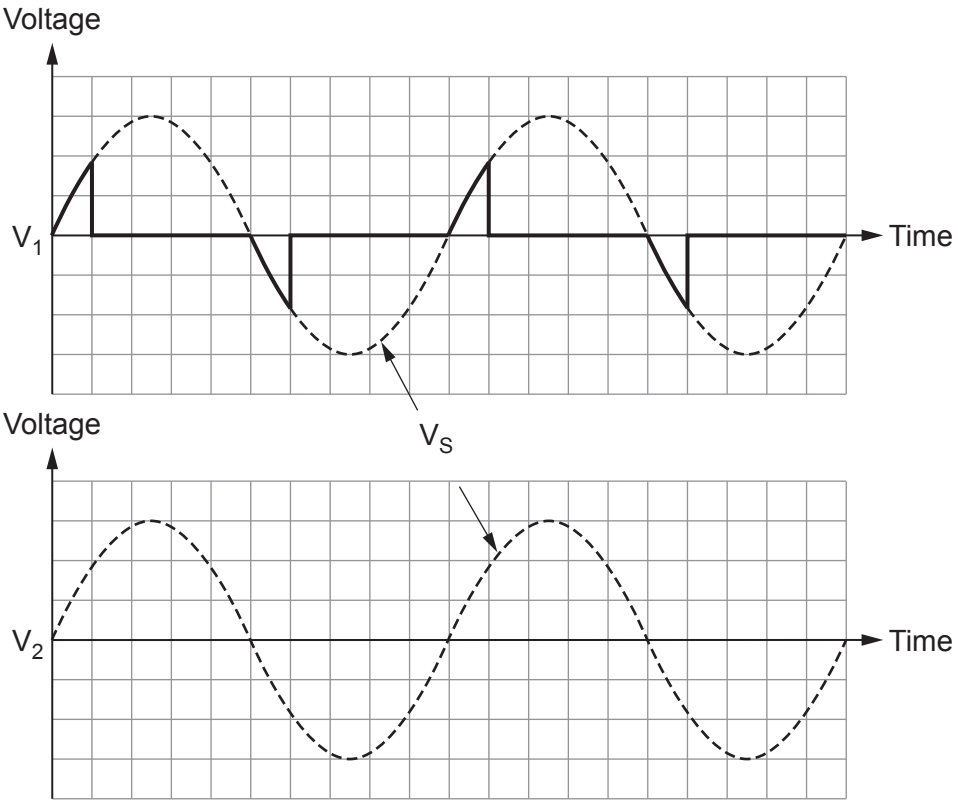
component P .....

component Q ..... [2]

(iii) The phase shift is set to zero. The upper graph shows voltage $V_1$. The AC supply $V_S$ is shown as a dashed line.

I. Use the lower axes to sketch the voltage $V_2$, across the lamp. [2]

II. Add an arrow, labelled X, to show a time when the lamp is at its brightest. [1]




**END OF PAPER**

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| Question number | Additional page, if required.<br>Write the question number(s) in the left-hand margin. |
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GCE A LEVEL

A490U20-1A

S23-A490U20-1A

**FRIDAY, 9 JUNE 2023 – AFTERNOON**

# ELECTRONICS – A level component 2

# Data Booklet

A clean copy of this booklet should be issued to candidates for their use during each A Level Electronics examination.

Centres are asked to issue this booklet to candidates at the start of the A Level Electronics course to enable them to become familiar with its contents and layout.

A490U201A
01

## Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

## Standard Multipliers

| Prefix | Multiplier |
|---|---|
| T | $\times 10^{12}$ |
| G | $\times 10^{9}$ |
| M | $\times 10^{6}$ |
| k | $\times 10^{3}$ |

| Prefix | Multiplier |
|---|---|
| m | $\times 10^{-3}$ |
| μ | $\times 10^{-6}$ |
| n | $\times 10^{-9}$ |
| p | $\times 10^{-12}$ |

## Useful equations

$$C = \frac{Q}{V}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$C = \frac{C_1 C_2}{C_1 + C_2}$$

$$C = C_1 + C_2$$

$$V_{rms} = \frac{V_0}{\sqrt{2}}$$

$$I_{rms} = \frac{I_0}{\sqrt{2}}$$

$$I_C = h_{FE} I_B$$

$$I_D = g_M (V_{GS} - 3)$$

$$P = I_D^2 r_{DSon}$$

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B + 1) = A$$

 

$$G = \frac{V_{OUT}}{V_{IN}}$$

$$G = 1 + \frac{R_F}{R_I}$$

$$G = -\frac{R_F}{R_{IN}}$$

$$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + ....\right)$$

$V_{OUT} = V_S$ for $V_+ > V_-$

$V_{OUT} = -V_S$ for $V_+ < V_-$

$V_{OUT} = V_{IN}$

$$\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

$$\text{slew rate} = 2\pi f V_P$$

$$\text{resolution} = \frac{\text{i/p voltage range}}{2^n}$$

$$X_C = \frac{1}{2\pi f C}$$

$$X_L = 2\pi f L$$

$$Z = \sqrt{R^2 + X^2}$$

$$f_0 = \frac{1}{2\pi\sqrt{L\,C}}$$

$$R_D = \frac{L}{r_L C}$$

$$Q = \frac{f_0}{\text{bandwidth}} = \frac{2\pi f_0 L}{r_L}$$

$$N_{CH} = \frac{\text{available bandwidth}}{\text{channel bandwidth}}$$

$$\text{maximum data rate} = 2 \times \text{available bandwidth}$$

$$G_{dB} = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

$$SNR_{dB} = 10\log_{10}\frac{P_S}{P_N} = 20\log_{10}\frac{V_S}{V_N}$$

$$m = \frac{(V_{max} - V_{min})}{(V_{max} + V_{min})} \times 100\%$$

$$\beta = \frac{\Delta f_c}{f_i}$$

$$\text{bandwidth} = 2(\Delta f_0 + f_i) = 2(1+\beta) f_i$$

$$c = f\lambda$$

$$V_{OUT} = V_{DIFF}\left(\frac{R_F}{R_1}\right)$$

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**Turn over.**

$$T = RC$$

$$V_C = V_0\left(1 - e^{-\frac{t}{RC}}\right)$$

$$V_C = V_0 e^{-\frac{t}{RC}}$$

$$t = -RC\ln\left(1 - \frac{V_C}{V_0}\right)$$

$$t = -RC\ln\left(\frac{V_C}{V_0}\right)$$

$$f \approx \frac{1}{RC}$$

$$f = \frac{1}{T}$$

$$T = 1.1RC$$

$$t_H = 0.7(R_1 + R_2)C$$

$$t_L = 0.7R_2C$$

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

$$\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$$

$$V_r = \frac{I}{f_r C}$$

$$V_L \approx V_Z\left(1 + \frac{R_F}{R_1}\right)$$

$$\phi = \tan^{-1}\left(\frac{R}{X_C}\right)$$

$$f_b = \frac{1}{2\pi R C}$$

$$V_{OUT} \approx V_{IN} - 0.7$$

$$V_{OUT} \approx V_{IN} - 3$$

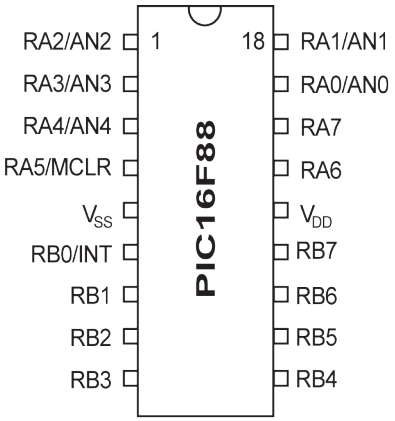
$$P_{MAX} = \frac{V_S^{\,2}}{8R_L}$$

## PIC Information

The PIC programs include 'equate' statements that define the following labels:

| Label | Description |
|---|---|
| PORTA | input / output port A |
| PORTB | input / output port B |
| TRISA | the control register for port A |
| TRISB | the control register for port B |
| STATUS | the status register |
| INTCON | the interrupt control register |
| W | Destination d = W, result stored in working register |
| F | Destination d = F, result stored in specified file register |
| RP0 | the register page selection bit 0 |
| Z | the zero flag status bit |
| GIE | the global interrupt controller bit |
| INT0IE | the external interrupt enable bit |

**Pinout for 16F88 PIC IC:**




## List of commands

| Mnemonic | Operands | Description |
|---|---|---|
| addlw | k | Add working register to literal k |
| andlw | k | AND working register with literal k |
| bcf | f, b | Clear bit b of file register f |
| bsf | f, b | Set bit b of file register f |
| btfsc | f, b | Bit test bit b of file register f, skip if clear |
| btfss | f, b | Bit test bit b of file register f, skip if set |
| call | label | Call subroutine at label |
| clrf | f | Clear file register f |
| comf | f, d | Complement file register f |
| decfsz | f, d | Decrement file register f, skip if zero |
| goto | label | Unconditional branch to label |
| incf | f, d | Increment file register f |
| iorlw | k | Inclusive OR working register with literal |
| movf | f, d | Move file register f |
| movlw | k | Move literal to working register |
| movwf | f | Move working register to file register f |
| nop | - | No operation |
| retfie | - | Return from interrupt service routine and set global interrupt enable bit GIE |
| return | - | Return from subroutine |
| sublw | k | Subtract W from literal |

## Number system notation

| | |
|---|---|
| Decimal | d'153' |
| Hex | h'99' |
| Binary | b'10011001' |

## Structure of the INTCON register

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| GIE | PEIE | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF |

## Structure of the STATUS register

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| IRP | RP1 | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |

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