

Surname	Centre Number	Candidate Number
First name(s)		2



GCE A LEVEL

A490U20-1



S24-A490U20-1



FRIDAY, 7 JUNE 2024 – AFTERNOON

ELECTRONICS – A level component 2

Application of Electronics

2 hours 45 minutes

For Examiner's use only		
Question	Maximum Mark	Mark Awarded
1.	16	
2.	12	
3.	15	
4.	15	
5.	15	
6.	10	
7.	6	
8.	14	
9.	20	
10.	11	
11.	6	
Total	140	

ADDITIONAL MATERIALS

You will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen. Do not use gel pen or correction fluid.

You may use a pencil for graphs and diagrams only.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

If you run out of space, use the additional page(s) at the back of the booklet, taking care to number the question(s) correctly.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in question **11**.



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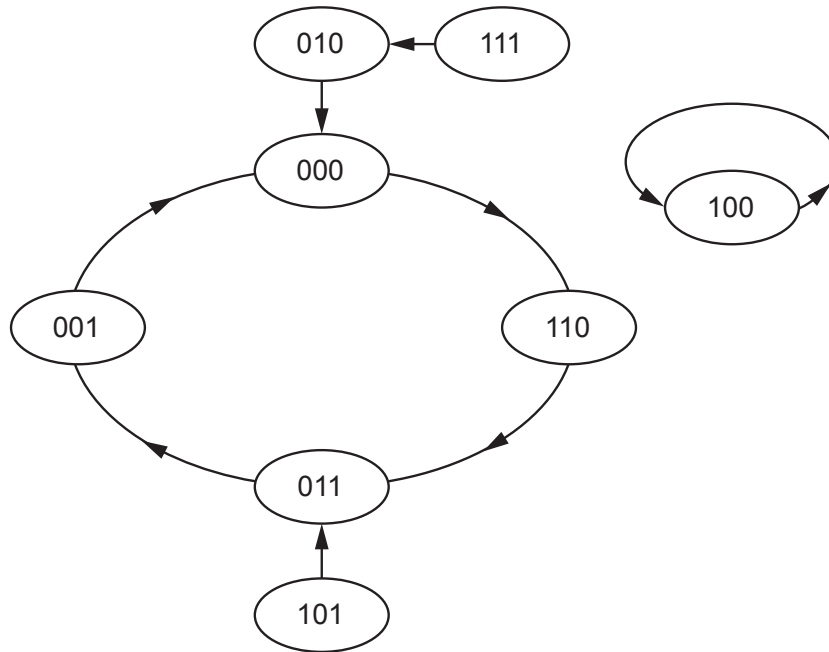
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Answer **all** questions.

1. (a) Here is the state diagram for a sequence generator.



(i) How many states are there in the main sequence for this sequence generator? [1]

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(ii) **Identify one unused state** that is not a stuck state by adding the letter 'X' next to it in the diagram. [1]

(iii) Use the state diagram to complete the truth table for this sequence generator. [3]

Current outputs			Next outputs		
C	B	A	D _C	D _B	D _A
0	0	0			



(i) **Add the correct clock connections** to the diagram opposite. [1]

(ii) Write down a Boolean equation for input D_A in terms of the outputs A, B and C. [2]

$D_A = \dots\dots\dots$

(iii) The signal at input D_B should be linked to the outputs by the equation:

$$D_B = B \cdot \bar{A} + \bar{B} \cdot A$$

Add logic gate(s) and connections to the circuit diagram opposite to generate this signal.

Credit will be given for using the minimum number of gates. [3]

(iv) The signal at input D_C should be linked to the outputs by the equation:

$$D_C = \overline{(C + B)} \cdot \bar{A}$$

Add logic gate(s) and connections to the circuit diagram opposite to generate this signal.

Credit will be given for using the minimum number of gates. [3]



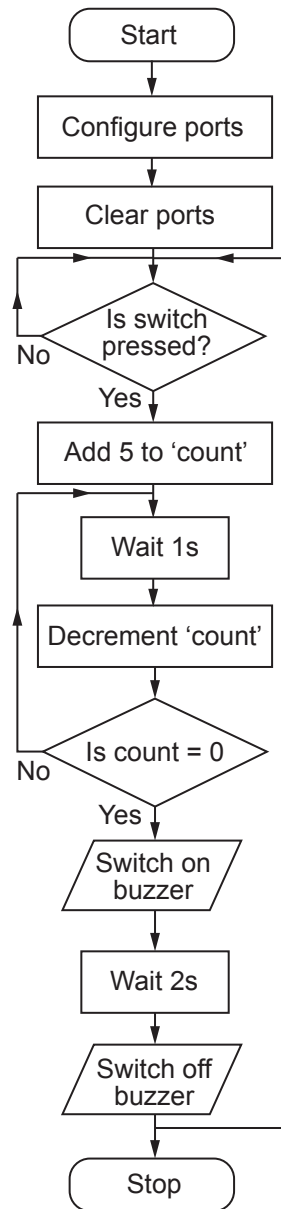
2. A student writes a microcontroller program that causes a 5 second delay after a switch is pressed. It then sounds a buzzer for a set time.

The program uses a one second delay subroutine, called 'onsec'.

The program is listed below and the flowchart is shown alongside:

```

124      bsf      STATUS,RP0
125      movlw   b'00000001'
126      movwf   TRISA
127      movlw   b'00000000'
128      movwf   TRISB
129      bcf      STATUS,RP0
130      clrf    PORTA
131      clrf    PORTB
132  test  btfss   PORTA,0
133      goto    test
134  start movlw   b'00000101'
135      movwf   count
136  next  call    onsec
137      decfsz  count,1
138      goto    next
139      bsf     PORTB,0
140      call    onsec
141      call    onsec
142      bcf     PORTB,0
143      goto    test
    
```



(a) What is the purpose of the instructions between lines 124 and 129? [1]

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(b) After the switch is pressed, how many times is the instruction in line 138 executed before the buzzer sounds? Explain your reasoning. [2]

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(c) Which port and which bit is the switch connected to? [2]

Port

Bit

(d) In which line does the microprocessor check to see if the switch has been pressed? [1]

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(e) Before the microcontroller executes the instruction in line 137, the 'count' register contains the number '3'. What does it contain after the instruction is executed? [1]

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(f) Explain in detail how the processor knows when the 'count' register contains zero. [3]

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(g) Modify **one** instruction so that the buzzer sounds 10s after the switch is pressed.

(i) What is the modified instruction? [1]

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(ii) At which line does this occur? [1]

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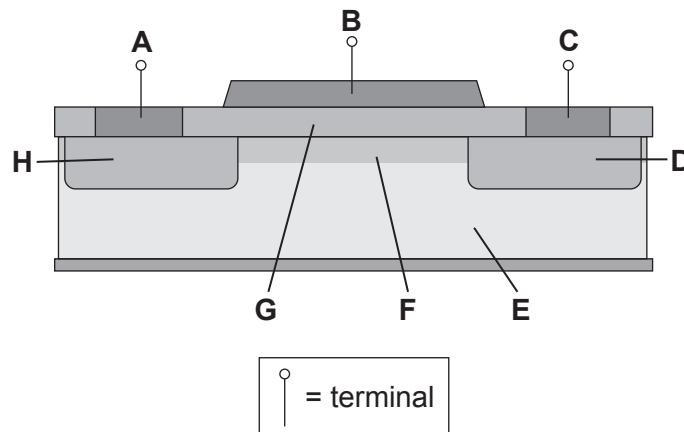


3. (a) Many electronic components rely on the properties of p-n junctions in semiconducting materials, some forward biased and some reverse biased.

Insert the word 'forward' or 'reverse' to complete each of the following statements: [2]

- (i) A LED gives off light when biased.
- (ii) A photodiode is used to detect light when biased.
- (iii) A silicon diode is used in bias to protect a transistor from back-emf.
- (iv) For a thyristor to conduct, the anode/cathode junction must be biased.

- (b) The following diagram shows the simplified structure of a MOSFET transistor when it is conducting:



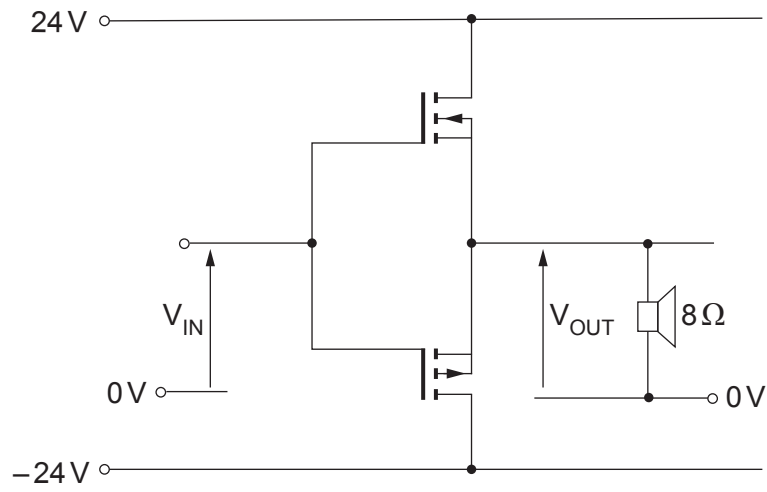
Which letter, **A** to **H**, identifies:

[3]

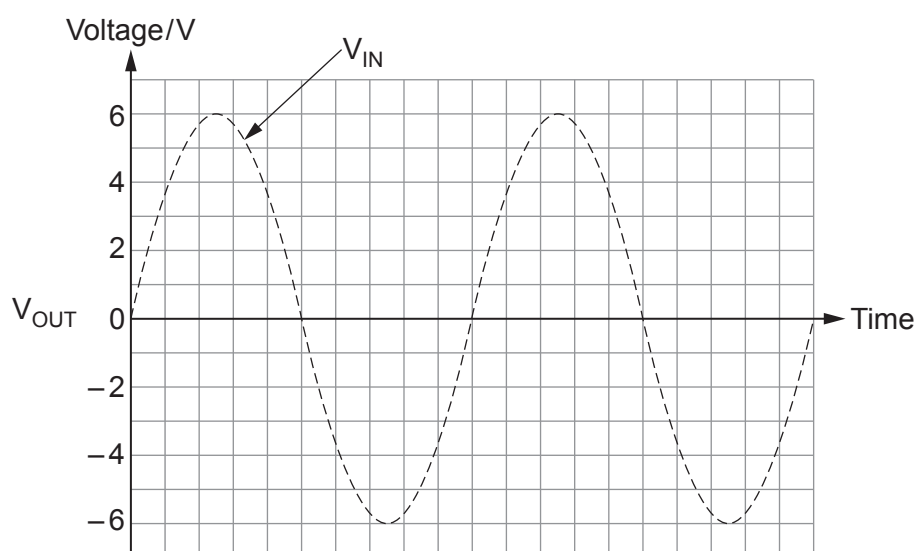
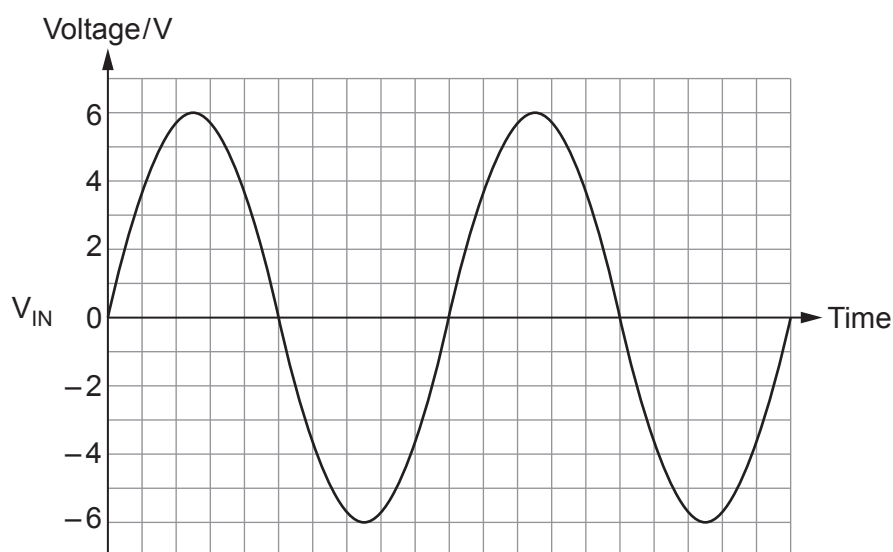
- (i) the gate terminal
- (ii) the conducting channel
- (iii) the insulator



- (c) The following diagram shows an n-channel and a p-channel MOSFET used in a push-pull power amplifier sub-system.



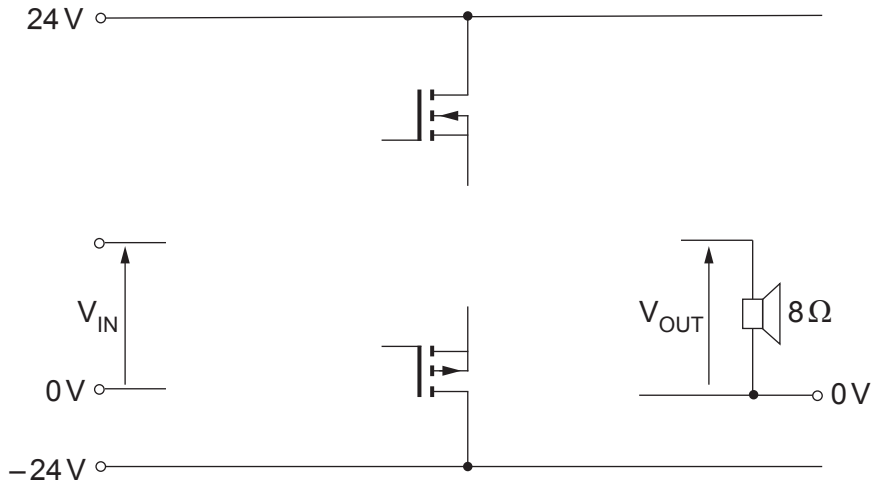
- (i) Use the axes provided to draw a graph showing the output voltage V_{OUT} produced by this sub-system when the input signal V_{IN} is applied. [3]



(ii) What is the name of the distortion produced by this sub-system? [1]

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(iii) Draw a modified circuit diagram for the sub-system showing how negative feedback can be used to remove this distortion. [3]



(iv) Calculate the maximum power output available from this modified sub-system. [3]

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4. (a) (i) Describe **one** advantage and **one** disadvantage of using optical fibre communication compared with free space microwave communication. [2]

Advantage:

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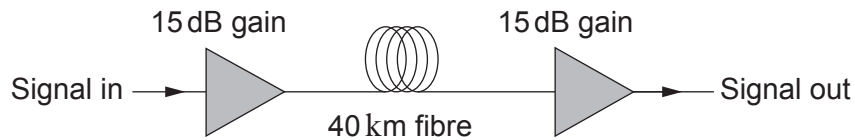
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Disadvantage:

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(ii) The diagram shows part of an optical fibre communication system.



A 40 km fibre optic cable, with a loss of 0.8 dB km^{-1} , connects the two regenerators.

Each regenerator produces a power gain of 15 dB.

Calculate the power delivered at the output of the system when the input power is 25 mW. [5]

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(b) TDM (time-division multiplexing) is used to transmit a number of identical PCM (pulse code modulation) channels along a single optical fibre communications link.

The specification for the PCM transmitters used in this link includes:

- sampling clock frequency = 20 kHz;
- PISO clock frequency = 5 MHz;
- sample levels defined by a 12-bit code.

(i) What is the highest signal frequency that these PCM transmitters can convert into digital form without distortion? [1]

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(ii) How many sampling levels are available using a 12-bit code? [2]

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(iii) How many of these PCM channels can be combined using TDM on this link? [5]

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A490U201
13

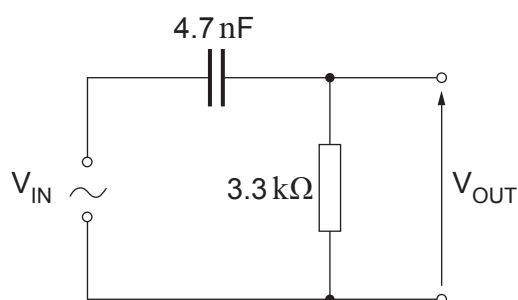


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5. For the high-pass passive filter shown in the following circuit, the input voltage, $V_{IN} = 15\text{ V}$.



- (a) The frequency of the AC voltage, V_{IN} , is 100 Hz.
At this frequency:

(i) Calculate the reactance of the capacitor. [2]

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(ii) Estimate the output voltage, V_{OUT} , of the filter.
Give a reason for your answer. [2]

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(b) Give **two** advantages of active filters over passive filters. [2]

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- (c) (i) Design an active treble cut filter with a break frequency of 2.1 kHz and a low frequency voltage gain of -25 , using a 0.1 nF capacitor. [5]

Justify your choice of component values by including appropriate calculations.

Complete the circuit diagram below.

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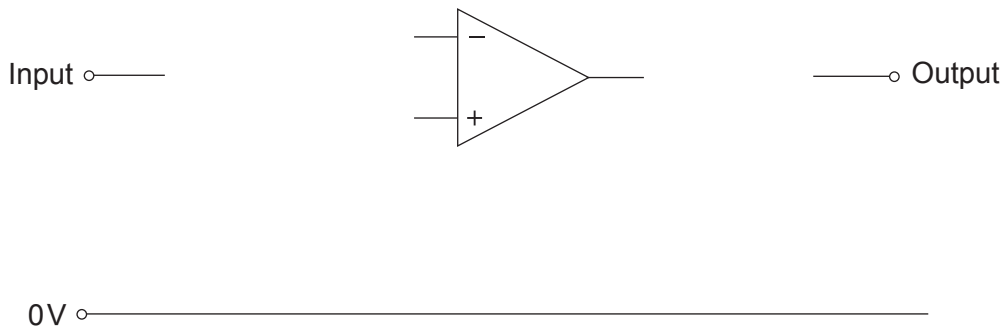
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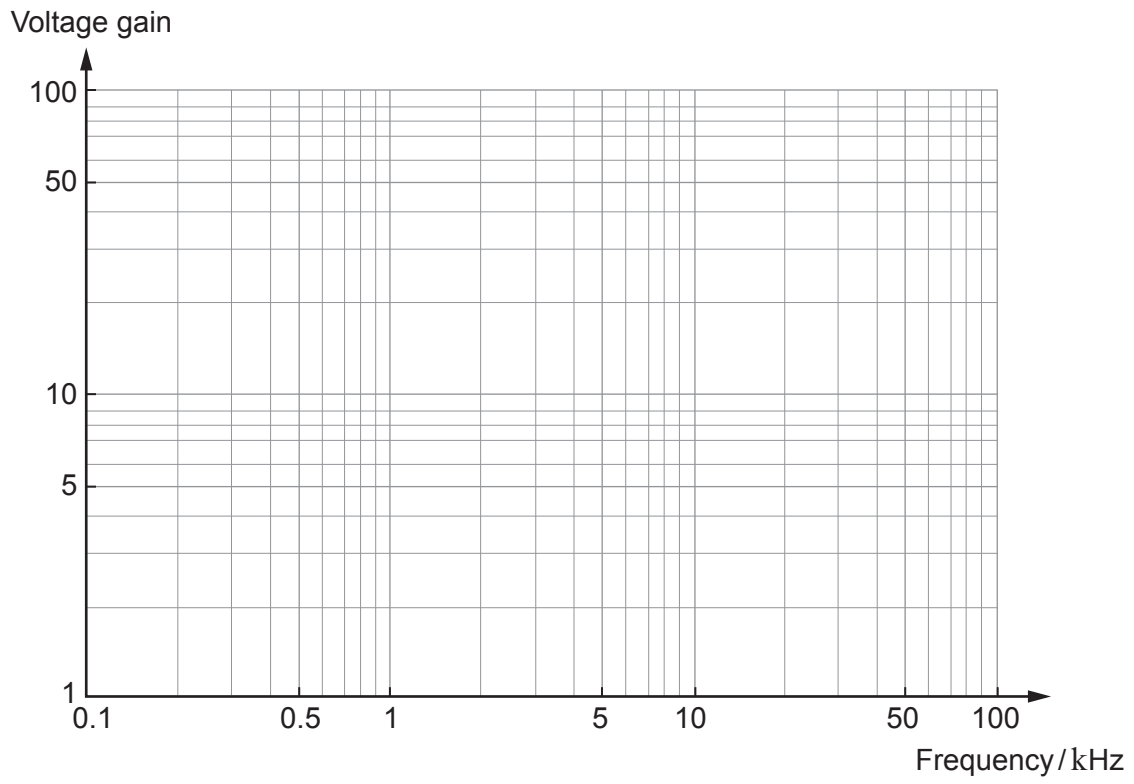
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(ii) Use the axes provided to sketch the frequency response of this filter.

[4]



A490U201
17

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6. Op-amps are used widely in public address systems.

(a) In preamplifiers, they are used as voltage amplifiers.

(i) Design a microphone preamplifier, using an op-amp with a gain-bandwidth-product of 5 MHz to meet the following specification: [5]

- input impedance > 1 M Ω ;
- bandwidth > 20 kHz;
- voltage gain = 100.

The microphone has an output impedance of 200 Ω .

Draw the circuit diagram for your design in the space below.

Justify your choice of component values by including appropriate calculations.

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(ii) Why is it important that the preamplifier has a high input impedance in this system? [2]

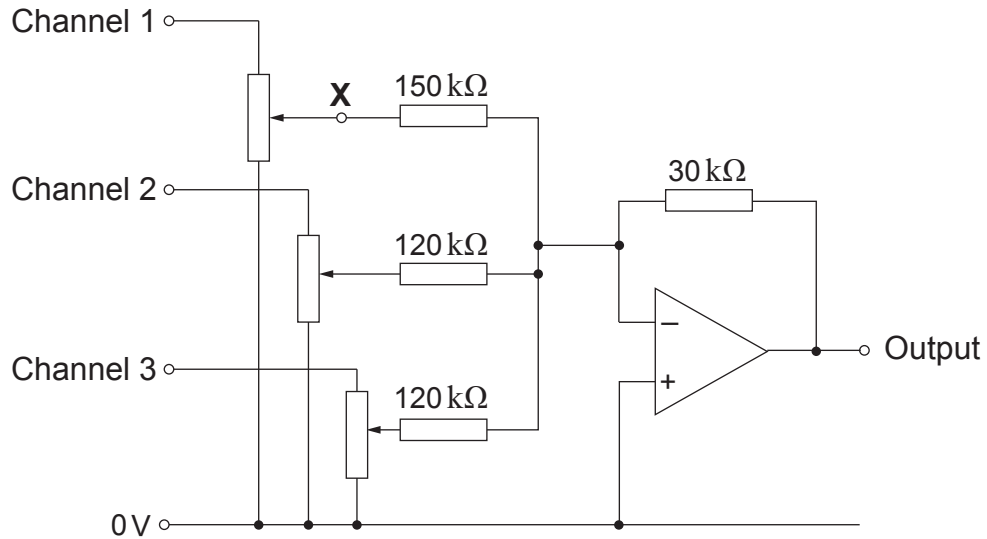
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(b) The mixer, shown in the following circuit diagram, also uses an op-amp voltage amplifier.



To test the mixer, three steady DC signals of +2V are applied to the input channels.

- (i) The potentiometer attached to Channel 1 is adjusted from one extreme to the other.
What range of voltages will result at point X?

Range of voltages at X is V to V [1]

- (ii) By adjusting the potentiometers on all three channels, the output voltage can be varied.
What is the maximum output voltage possible assuming the op-amp does not saturate? [2]

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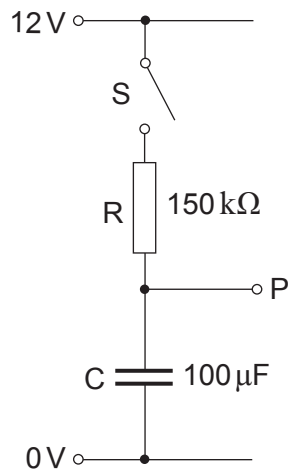
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Maximum output voltage = V



7. In the circuit shown below, the capacitor is initially uncharged.



- (a) Calculate the time constant for the RC network. [2]

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- (b) The switch is closed at time $t = 0$.

After how many seconds does the voltage at P reach 6V? [2]

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- (c) What are the limitations of this circuit as a practical timing sub-system? [2]

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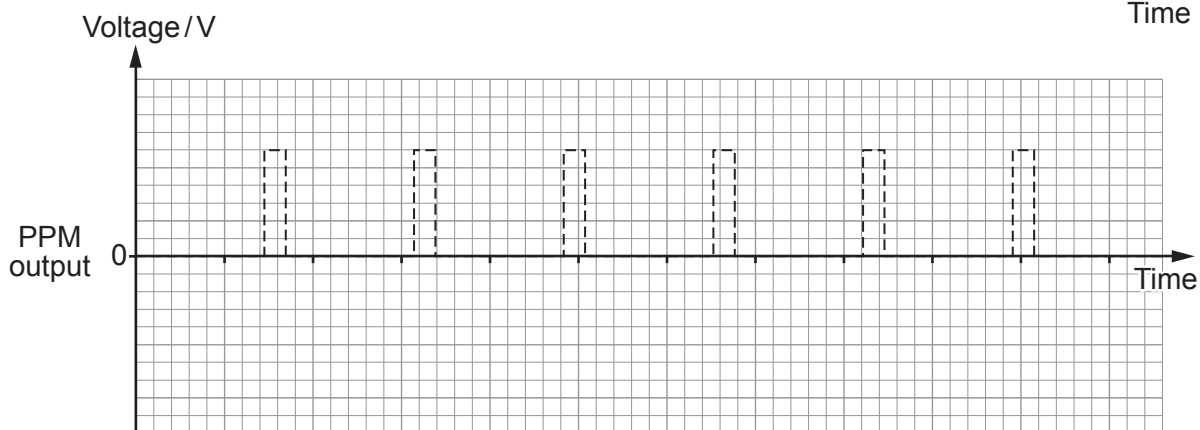
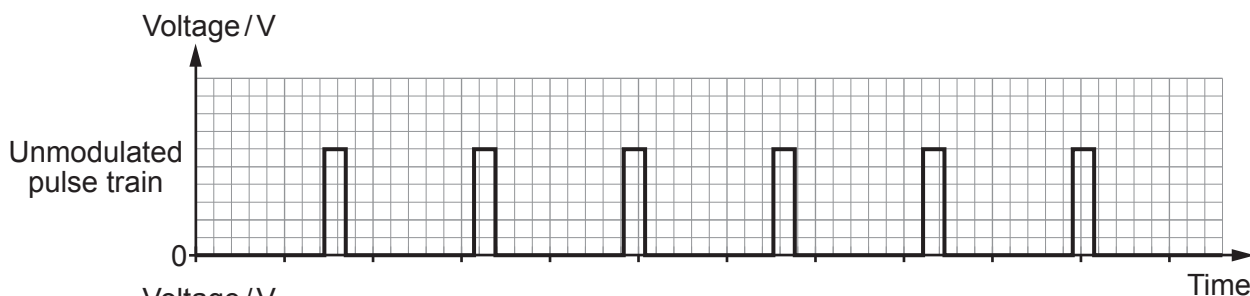
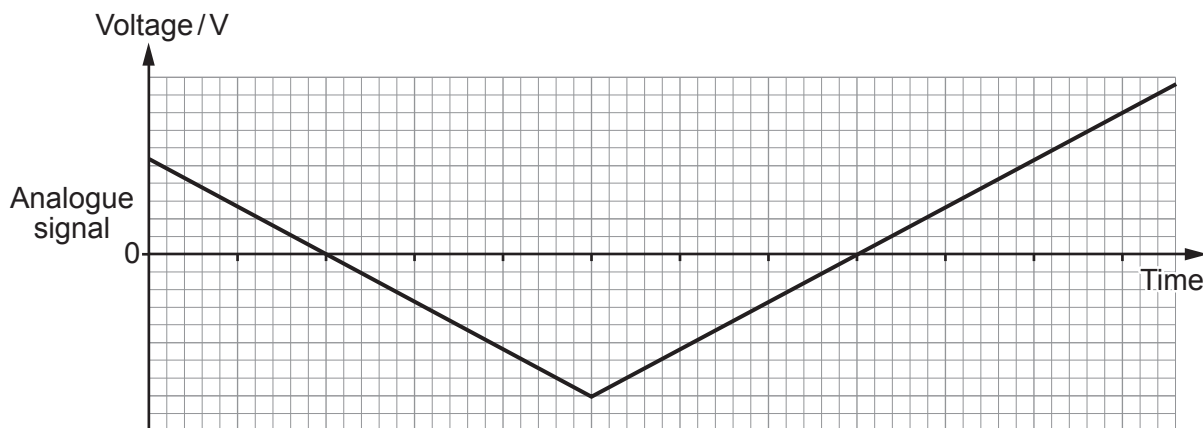


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8. (a) (i) In digital communication systems, analogue signals must be 'digitised'. One way to do this is to convert them into a PPM pulse train. Complete the graph below to show the PPM pulse train carrying the following analogue signal. [3]



- (ii) Why is a PPM signal affected less by interference than a PAM signal? [2]

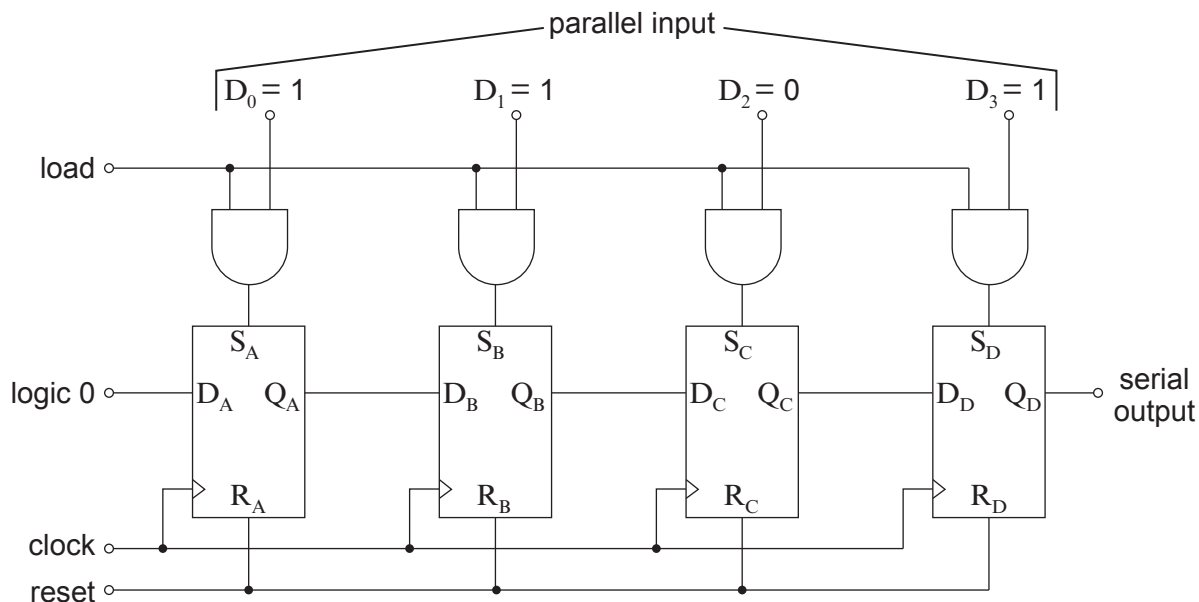
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- (b) The following diagram shows one form of PISO shift register used in digital communications.



The data word '1011' is presented to inputs D_3 to D_0 and the signals shown on the next page are applied to the 'load', 'clock' and 'reset' terminals.

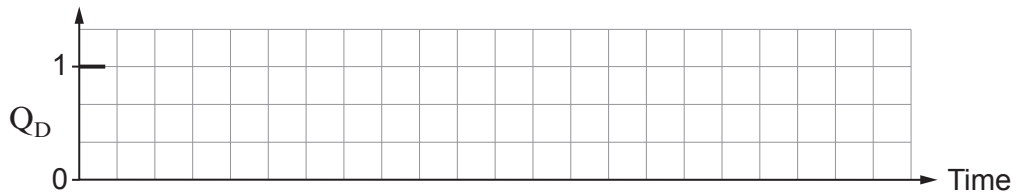
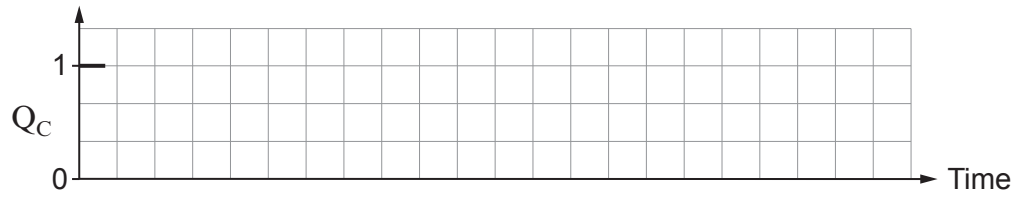
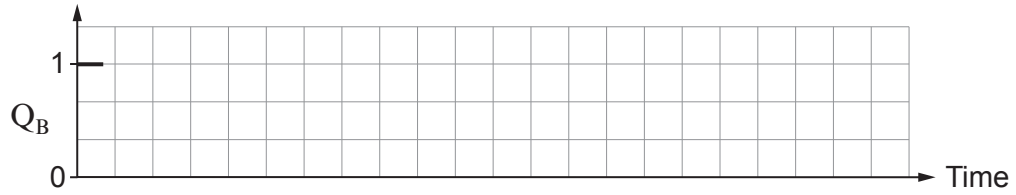
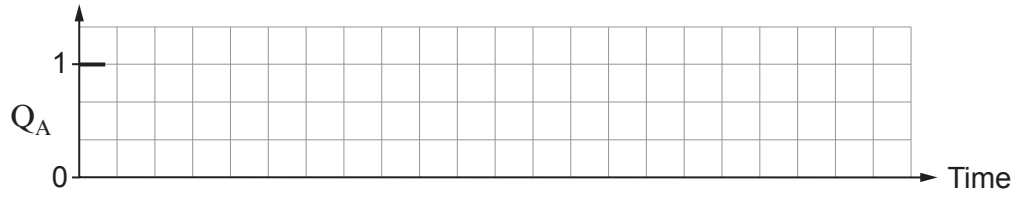
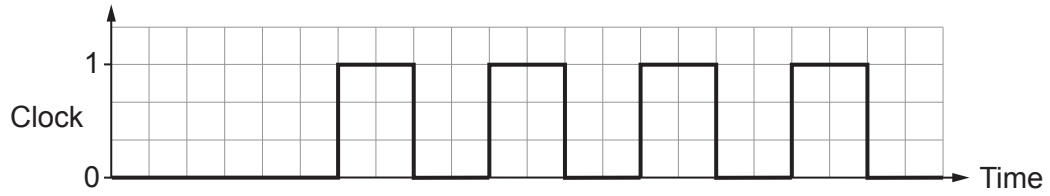
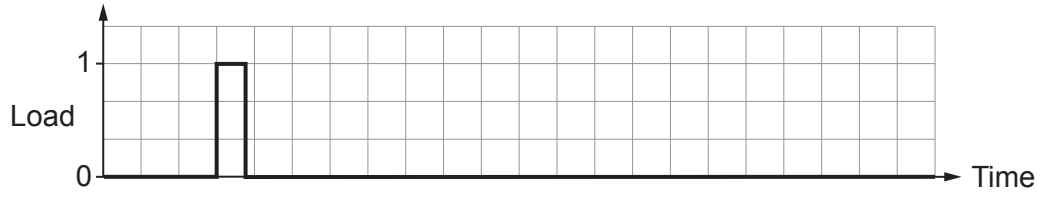
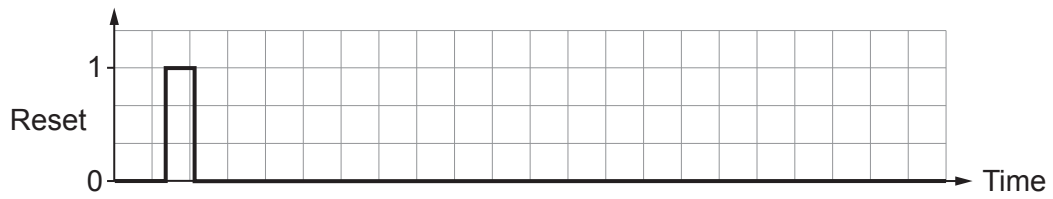
- (i) Convert the binary number '1011' to:

I. the equivalent decimal number [1]

II. the equivalent hexadecimal number [1]



(ii) Complete the graphs for Q_A , Q_B , Q_C and Q_D , showing the signals generated as a result. [5]



(iii) Refer to the graphs to explain how parallel-to-serial conversion is achieved. [2]

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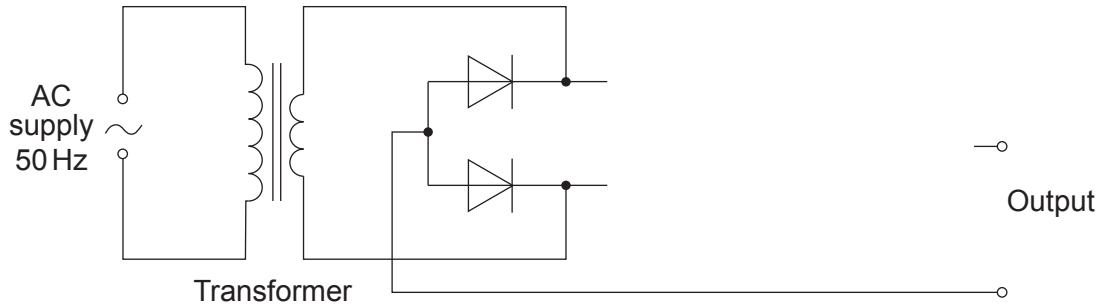
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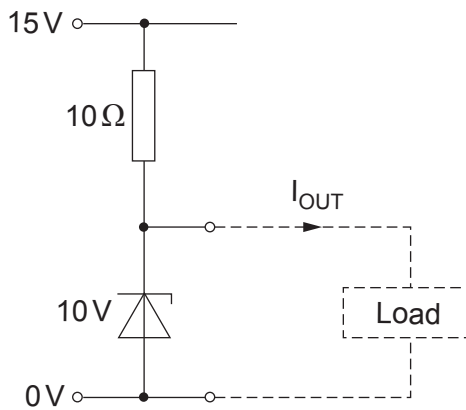


9. An engineer is designing a 10V regulated power supply, consisting of a full-wave rectifier, with smoothing, followed by a voltage regulator sub-system.

- (a) **Complete the following circuit diagram** for a full-wave rectifier sub-system, including a 2200 μF smoothing capacitor. Indicate clearly the polarity of the capacitor. [3]



- (b) The regulator sub-system is connected to a 15VDC supply for testing as shown in the following circuit diagram.



The zener diode requires a current of at least 10 mA to remain in reverse breakdown.

- (i) Calculate the maximum possible output current, I_{OUT} . [3]

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- (ii) Calculate the maximum power dissipated in the zener diode. [2]

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- (iii) Providing that the zener diode remains in reverse breakdown, the power dissipated in the $10\ \Omega$ resistor remains constant, regardless of the output current.

Explain why this is so. [1]

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- (c) The test 15 VDC supply is removed and the regulator is now connected to the output of the rectifier sub-system. The rectifier sub-system has a peak output of 15 V with no load connected.

- (i) Calculate the ripple voltage across the smoothing capacitor when the current through the $10\ \Omega$ resistor is at its maximum. [2]

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- (ii) Calculate the expected values for:

I. The minimum voltage across the $10\ \Omega$ resistor. [2]

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II. The minimum current through the $10\ \Omega$ resistor. [1]

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(iii) How would this affect the performance of the regulator? [2]

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(d) The circuit is modified by adding a transistor connected as an emitter follower to the output.

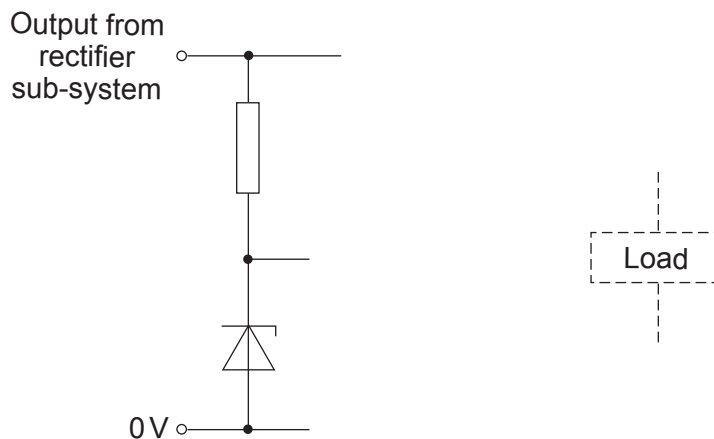
(i) What benefit does this modification bring to the power supply? [1]

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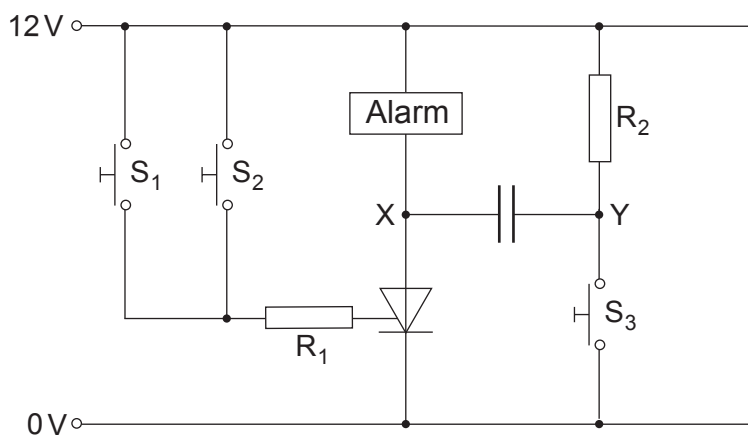
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(ii) Complete the following diagram to show this modification. No component values are required. [3]



10. The circuit in the next diagram shows part of a car alarm system.



(a) Describe the functions of switches S_1 , S_2 and S_3 in this system. [2]

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(b) What is the voltage at point X when: [2]

- (i) the alarm is turned off.
Voltage at X is V
- (ii) the alarm is turned on.
Voltage at X is V



(c) The table provides data about the thyristor.

Parameter	Value
Maximum forward current	20 A
Minimum gate current	20 mA
Holding current	30 mA
Gate trigger voltage	1.5 V
Peak reverse voltage	400 V

Use this data to calculate the maximum value of R_1 .

[2]

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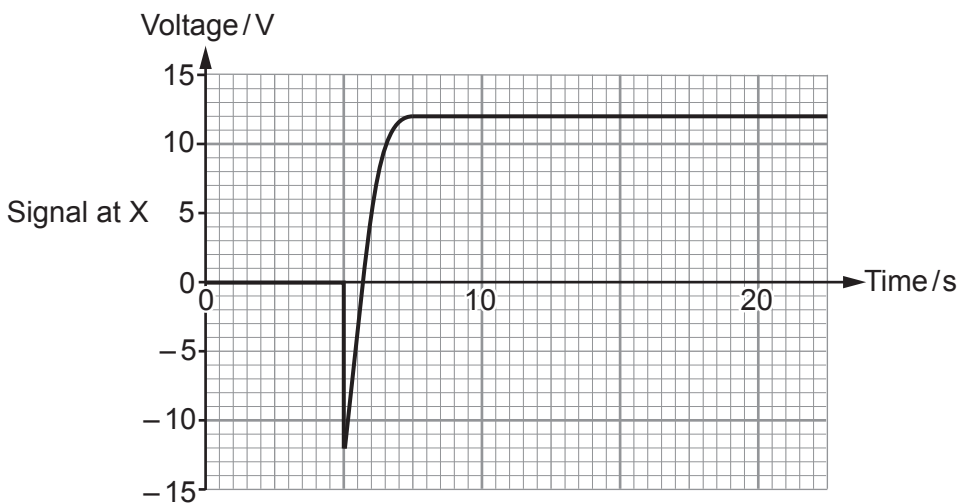
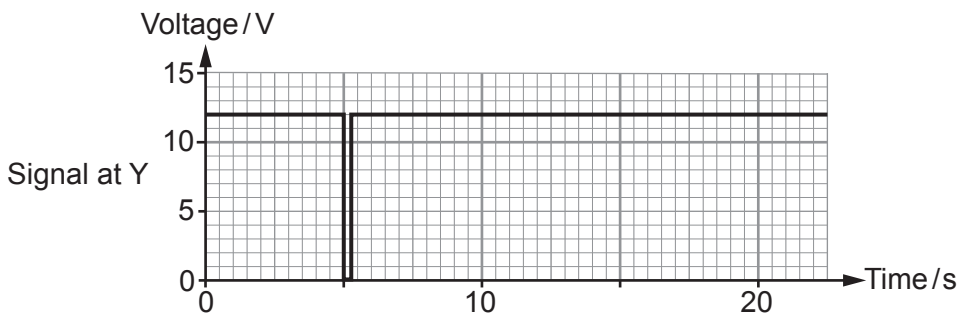
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(d) The graphs show signals obtained at points X and Y in the car alarm circuit.



(i) Describe what happened to produce the signal shown in the upper graph. [1]

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(ii) Explain what the lower graph shows. Include in your answer details about the states of the three switches and the alarm at various times. [4]

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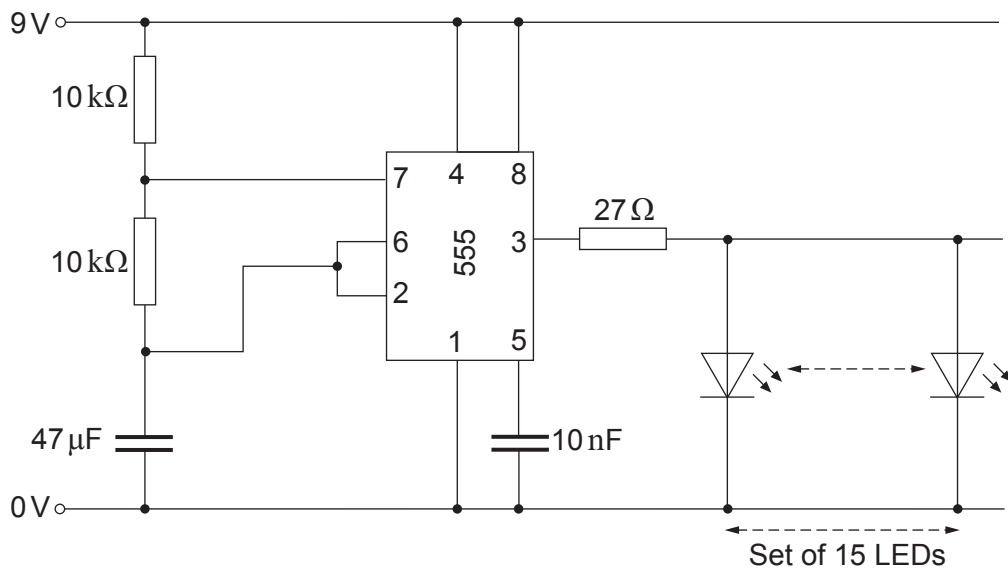


11. A student has designed an astable circuit, based on a 555 timer, to drive a set of Christmas tree LED lights.

The specification includes the following:

- the system is powered by a 9V PP3 rechargeable battery having a capacity of 600mAh;
- it controls a set of 15 miniature LEDs, each having a forward current of 12mA and forward voltage drop of 2V;
- the system will run continuously for at least 5 hours without the need for the battery to be recharged;
- the LEDs will flash at a frequency of about 1 Hz;
- to extend battery life, the astable output pulses with a mark:space ratio of 2:1;
- the 555 timer IC requires a supply current of 10mA and can source a current of 200mA;
- its high output voltage is 7V and its low output voltage is 0.5V.

The student's proposed circuit for the astable is shown below:



Evaluate the design using relevant calculations to determine if it meets the specification. Describe any modifications necessary.

[6 QER]

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