GCSE

4162/01

ELECTRONICS

UNIT E2 – Paper replacement test

P.M. WEDNESDAY, 17 June 2015

1 hour plus your additional time allowance

Surname _____

Other Names _____

Centre Number _____

Candidate Number 0 _____

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	2	
2.	2	
3.	4	
4.	3	
5.	3	
6.	5	
7.	3	
8.	2	
9.	5	
10.	5	
11.	5	
12.	5	
13.	2	
14.	5	
15.	6	
16.	3	
Total	60	

ADDITIONAL MATERIALS

In addition to this paper you may require a calculator and a ruler and separate insert.

INSTRUCTIONS TO CANDIDATES

Use black ink, black ball-point pen or your usual method.

Write your name, centre number and candidate number in the spaces provided on the front cover.

Answer ALL questions in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

Answer ALL questions.

1(a) An electronic system is designed to make a car indicator flash on and off continuously. Which of the following sub-systems is needed? (Tick (✓) the correct answer.) [1]

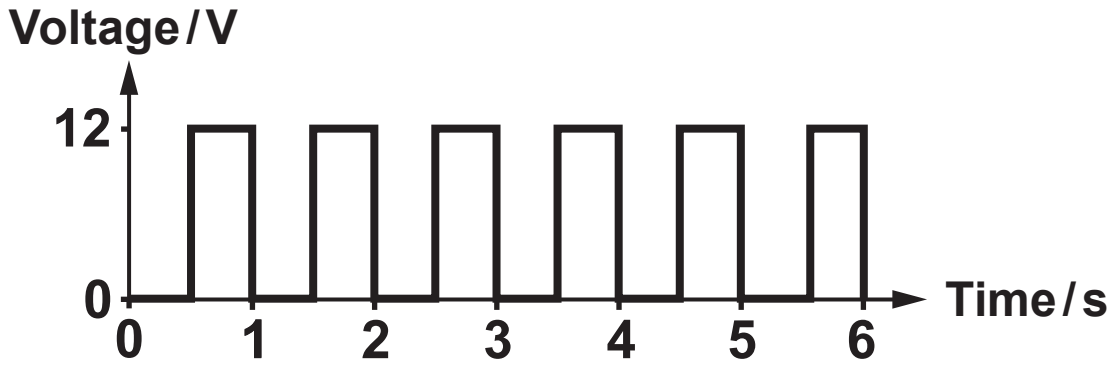
Monostable ☐

D-type flip-flop ☐

Astable ☐

Decade counter ☐

1(b) What is the time period of the signal shown here? (Tick (✓) the correct answer.) [1]



0.5 s ☐

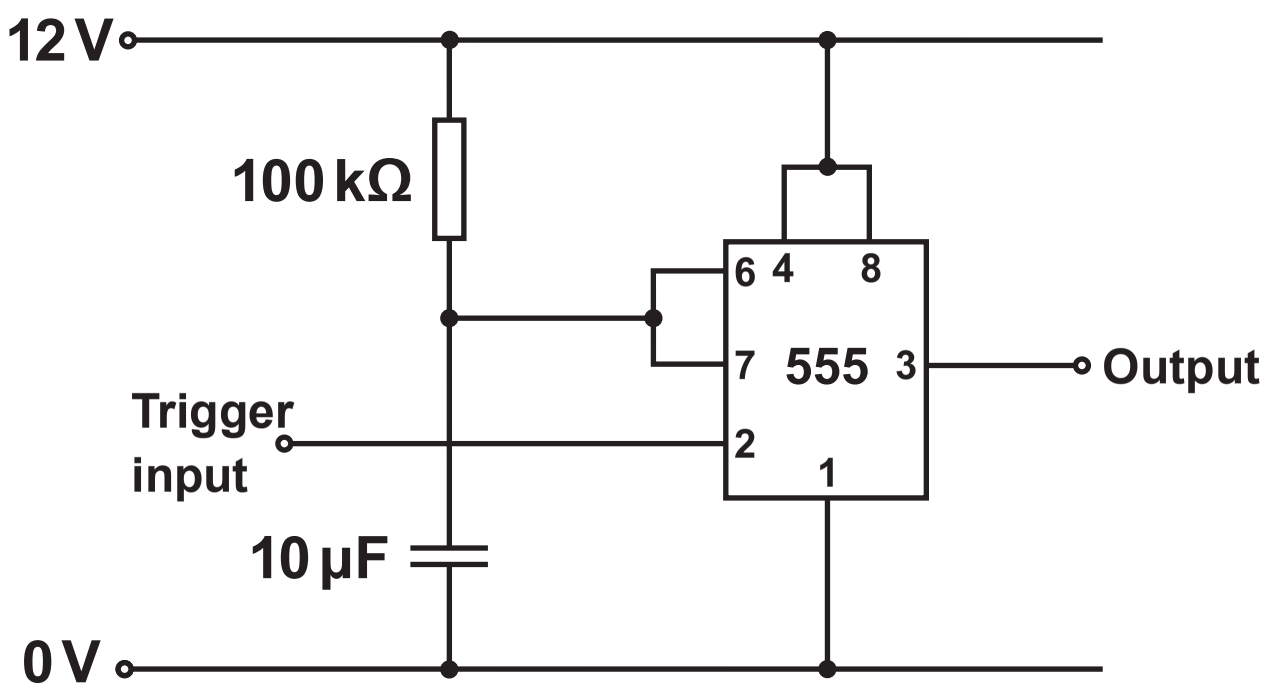
1 s ☐

2 s ☐

6 s ☐

12 s ☐

	Resistor	Capacitor
	10 kΩ	100 µF
	200 kΩ	10 µF
	100 kΩ	20 µF
	10 kΩ	10 µF



2. The circuit shown opposite produces a delay of 1.1 seconds.

(a) Which other resistor-capacitor pair will also produce a delay of 1.1 seconds?
(Tick (✓) the correct answer on the page opposite.)
[1]

1 s ☐

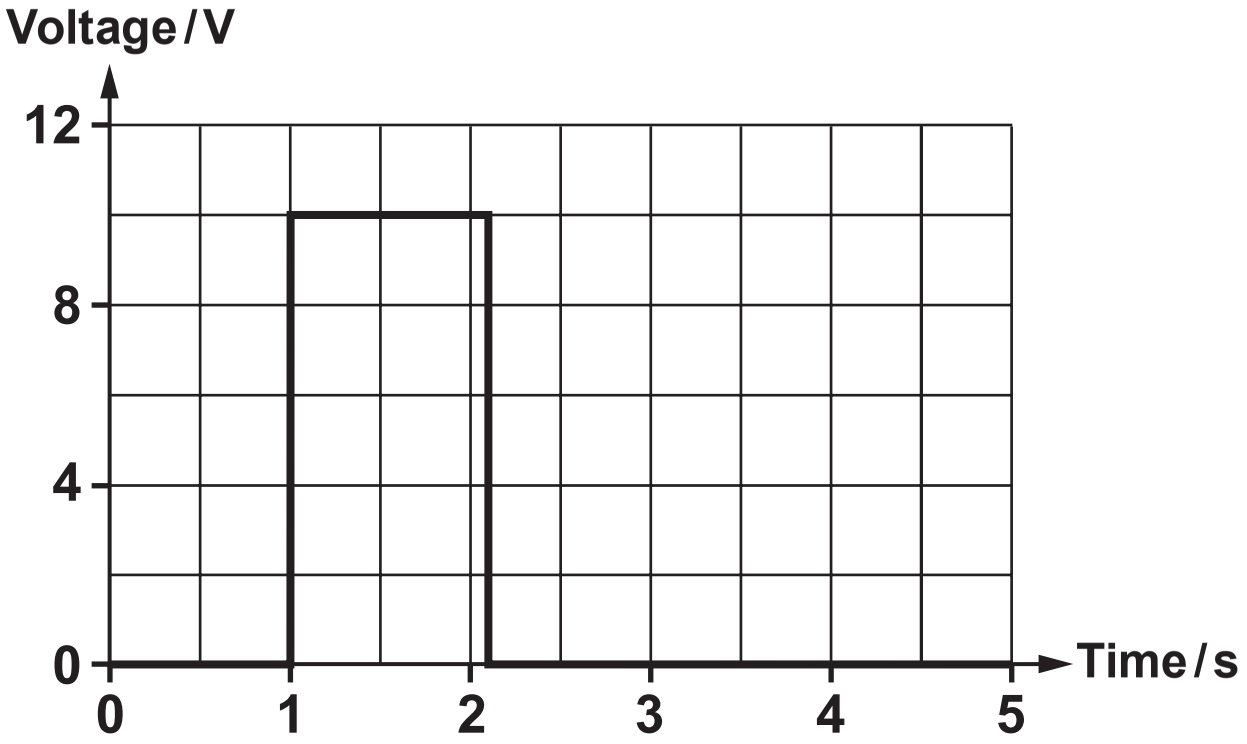
1.1 s ☐

2.1 s ☐

0 V ☐

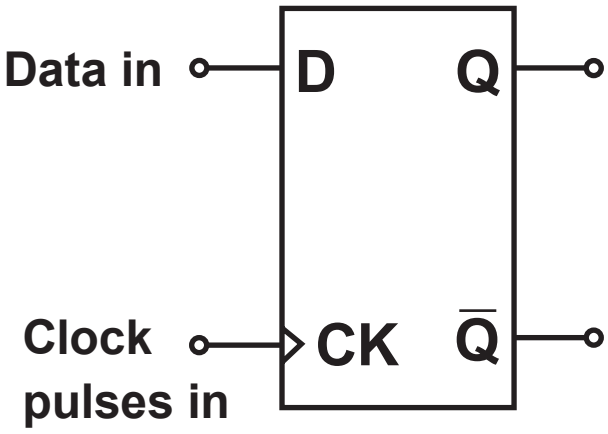
10 V ☐

12 V ☐



2(b) What is the amplitude of the output signal shown in the graph opposite?
(Tick (✓) the correct answer on the page opposite.)
[1]

3(a) Which of the following statements describes the action of the rising-edge triggered D-type flip-flop? (Tick (✓) the correct answer.) [1]



When the clock signal rises from logic 0 to logic 1:

Q stays at logic 1 ☐

$\overline{Q}$ stays at logic 1 ☐

Q outputs the logic state of the clock input ☐

$\overline{Q}$ outputs the logic state of the clock input ☐

Q outputs the logic state of the data input ☐

$\overline{Q}$ outputs the logic state of the data input ☐

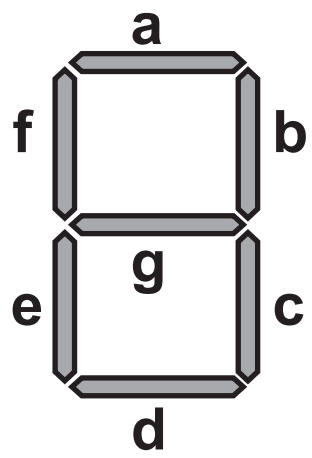
3(b) **The D-type flip-flop receives the clock and data signals shown in the graphs opposite. Complete the graphs to show the Q and $\overline{Q}$ outputs. [3]**

4. The diagram shows a 7-segment display.

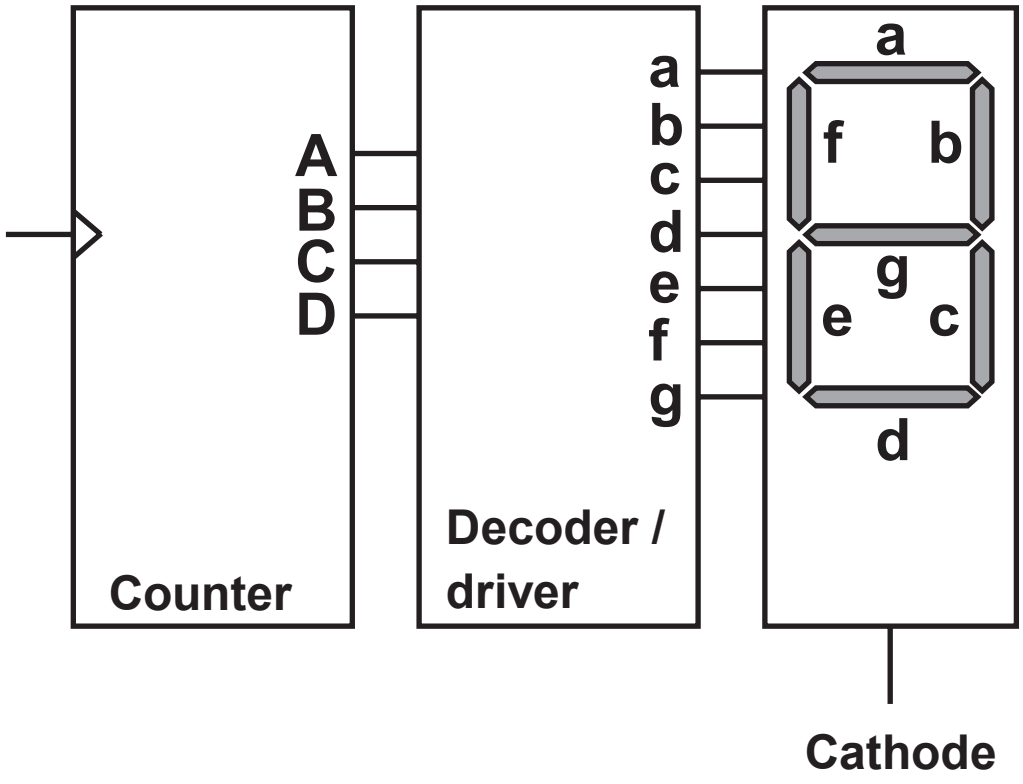
A logic 1 input signal makes a segment light up.

(a) Identify the number shown on the display when the signals given below are sent to the 7-segment display. [1]

SEGMENTS						
a	b	c	d	e	f	g
1	1	1	1	0	0	1



Number displayed is _____


A
B
C
D
Counter
a
b
c
d
e
f
g
Decoder /
driver
a
f
b
g
e
c
d
Cathode

4(b) **This display is used in a single digit decimal counting system, as the diagram opposite shows.**

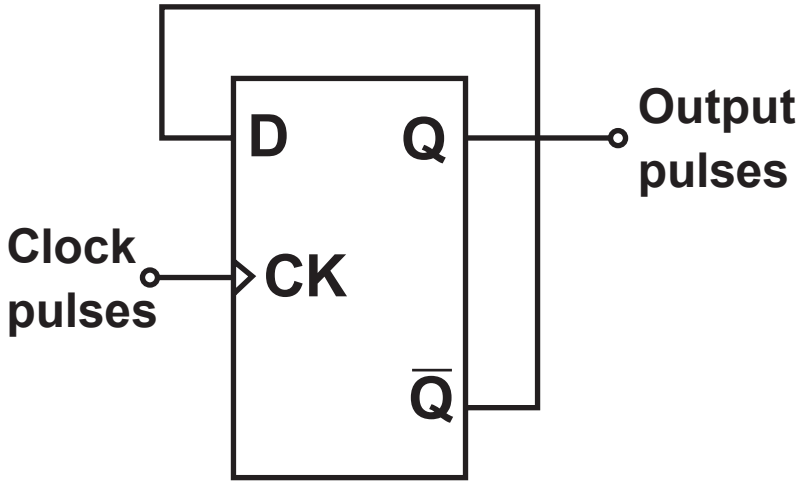
(i) **Select the row of the following table that creates the number '0' on the display. (Tick (✓) the correct answer.) [1]**

DECODER / DRIVER OUTPUTS							
a	**b**	**c**	**d**	**e**	**f**	**g**	
0	**0**	**0**	**0**	**0**	**0**	**1**	
0	**1**	**1**	**1**	**1**	**1**	**1**	
1	**1**	**1**	**1**	**1**	**1**	**0**	
1	**0**	**0**	**0**	**0**	**0**	**0**	

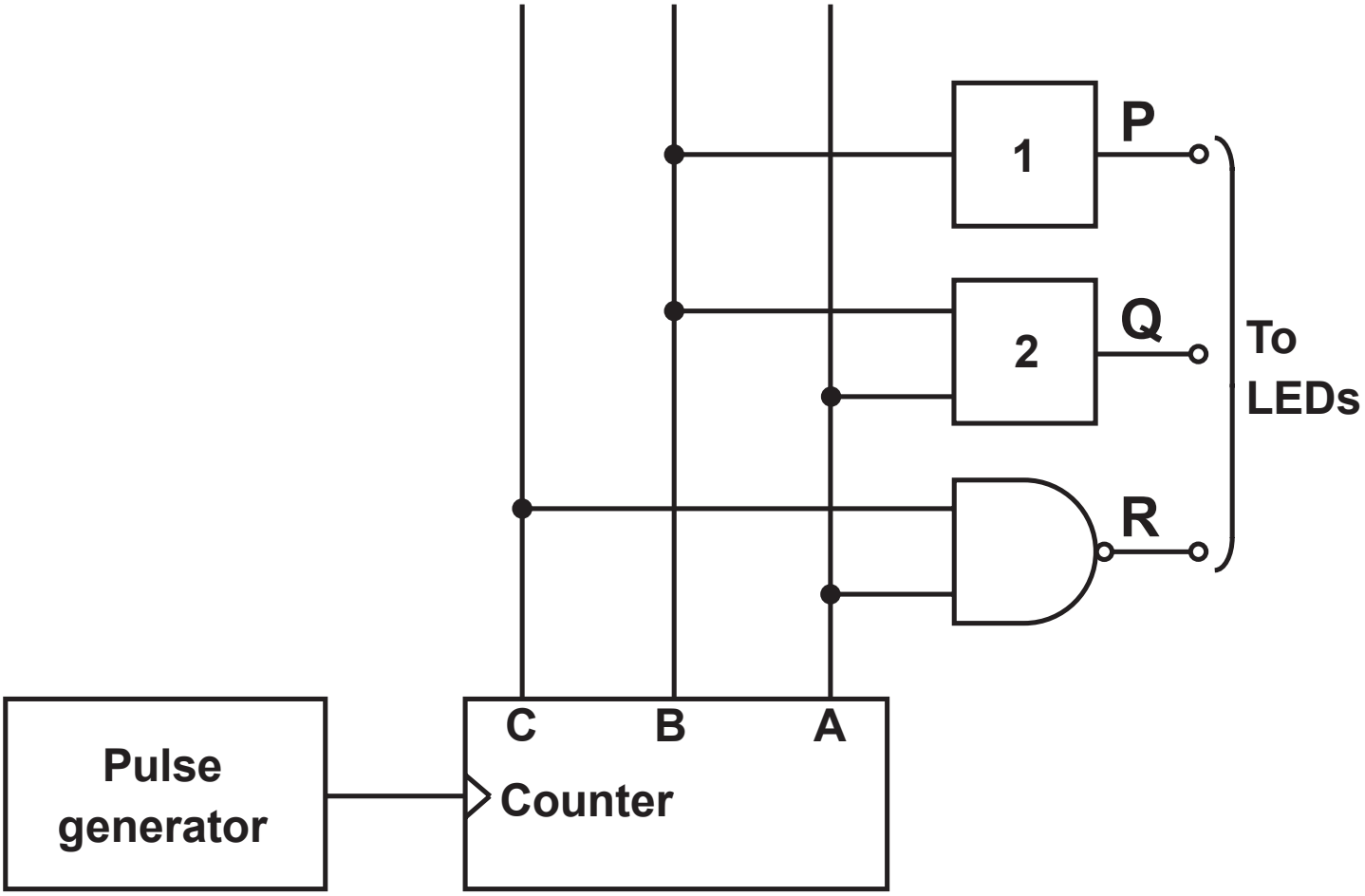
(ii) **What connection must be made to the cathode to make the display work? Connect the cathode to: (Circle the correct answer.) [1]**

5 V **0 V** **system reset** **clock input**

5. **The diagram below shows a rising-edge triggered D-type flip-flop set up as a one-bit counter.**



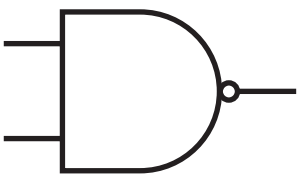
The top graph opposite shows the clock pulses applied to the counter.
Complete the graphs for Q and $\overline{Q}$. **[3]**

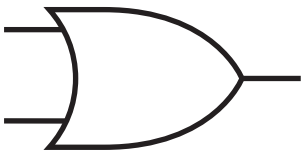


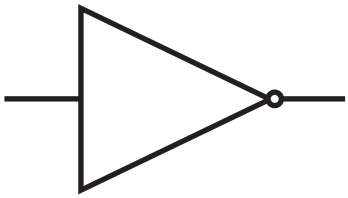
PULSE	COUNTER OUTPUTS			OUTPUTS TO LEDs	
	C	B	A	P	Q
0	0	0	0	1	0
1	0	0	1	1	0
2	0	1	0	0	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	1	0
6	1	1	0	0	0
7	1	1	1	0	1

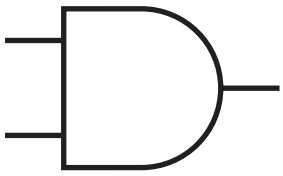
6. **The diagram opposite shows part of a light sequence controller circuit. Boxes 1 and 2 contain logic gates.**
The truth table is shown opposite.

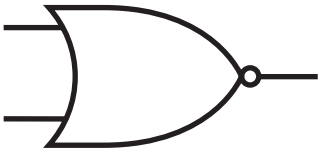
(a) **Select the logic gate, for box 1 to control output P as shown in the table opposite.**
(Circle the correct answer.) [1]



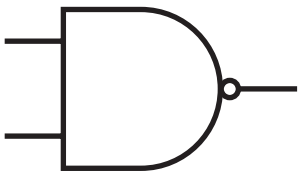


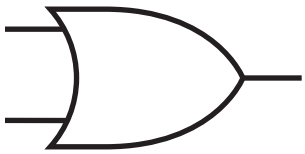


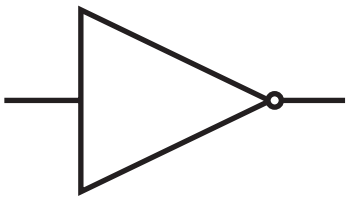


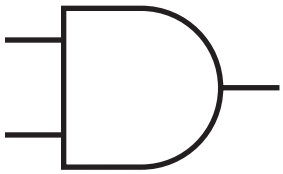


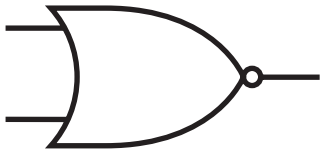
6(b) Select the logic gate, for box 2 to control output Q as shown in the table opposite page 13. (Circle the correct answer.) [1]











6(c) **The effect of the pulses is given in the table opposite page 13.**
Which two pulses cause output R to go to logic 0?
(Tick (✓) the correct answers.) [2]

PULSES

0 ☐

1 ☐

2 ☐

3 ☐

4 ☐

5 ☐

6 ☐

7 ☐

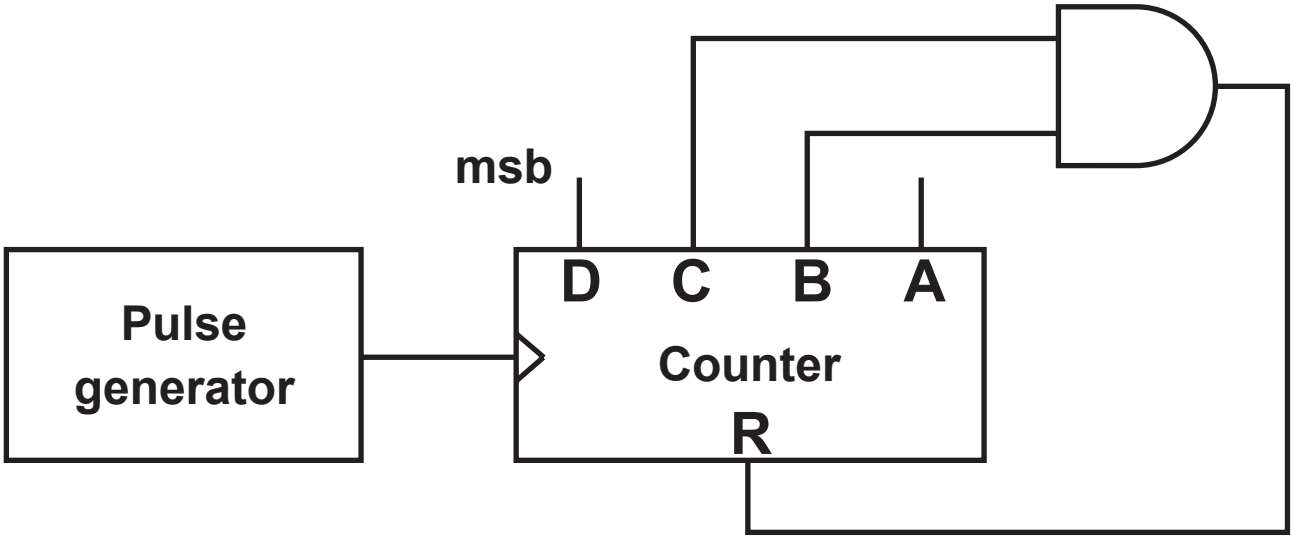
6(d) **The pulse generator has a period of 2 s. What is its frequency in Hz?**
(Tick (✓) the correct answer.) **[1]**

0.5 ☐

1.0 ☐

1.5 ☐

2.0 ☐



CLOCK PULSES RECEIVED	OUTPUTS				
	D	C	B	A	
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	

7. **The table opposite shows the initial sequence of output signals from a 4-bit counter.**

(a) **How many clock pulses are needed to produce the following outputs? [1]**

OUTPUTS			
D	**C**	**B**	**A**
0	**0**	**1**	**1**

Answer _____

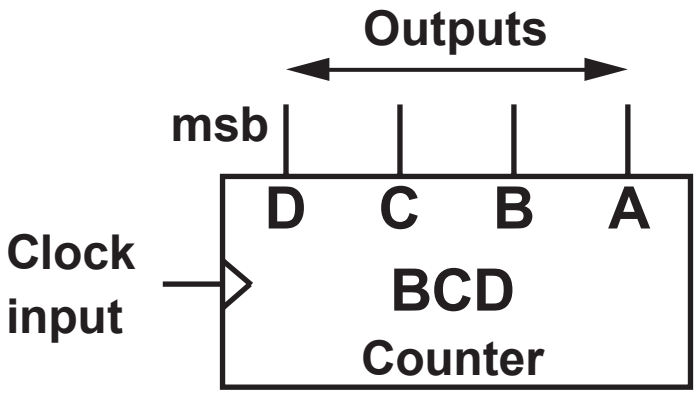
7(b) Select the correct output combination after four clock pulses.
(Tick (✓) the correct answer.) [1]

CLOCK PULSES RECEIVED	OUTPUTS				
	D	C	B	A	
4	0	1	0	1	
4	0	1	1	0	
4	0	1	0	0	
4	1	0	1	0	

7(c) **The counter resets when the Reset input, R, receives a logic 1 signal.**
Select the output combination that resets the counter. (Tick (✓) the correct answer.) [1]

OUTPUTS				
D	C	B	A	
0	1	0	1	
0	1	1	1	
0	1	1	0	
1	1	0	0	

8(a) Which combination causes the BCD counter to reset automatically?
(Tick (✓) the correct answer.) [1]



OUTPUTS				
D	C	B	A	
0	0	0	0	
1	1	1	1	
0	1	0	1	
1	0	1	0	

8(b) Which of the following output combinations will never occur in a BCD counter?
(Tick (✓) the correct answer.) [1]

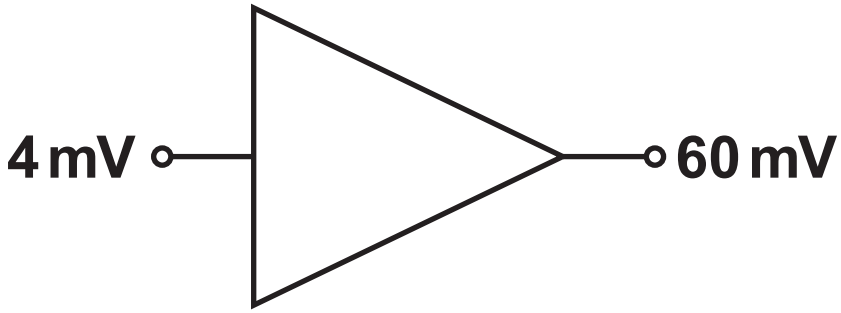
OUTPUTS				
D	**C**	**B**	**A**	
0	0	0	0	
0	1	1	1	
1	0	0	0	
1	1	0	0	

Microphone	
	Boosts the voltage from a signal source
Preamplifier	
Mixer	
	Turns sound into electrical signals
Power amplifier	
	Provides current to drive the output stage
Loudspeaker	

9(a) **Study the information opposite.**
The boxes on the left give the names of the sub-systems in a typical amplifier system.

The boxes on the right give the functions of three of these sub-systems.
Link EACH function to the correct sub-system. [3]

(b) **What is the voltage gain of the following preamplifier? [1]**



Answer _____

9(c) Complete the following statement.

A preamplifier requires a sufficiently high bandwidth in order to:
(Tick (✓) the correct answer.) [1]

make weak signals audible; ☐

overcome the effects of interference; ☐

amplify the required range of frequencies; ☐

limit the current drawn from the power supply. ☐

10. A non-inverting amplifier has a voltage gain of 6.

(a) The upper graph opposite shows the signal applied to the input of the amplifier.
Draw the signal in the lower graph opposite so that it shows the corresponding output signal. [2]

10(b) (i) Study the diagrams opposite. Which is the circuit diagram for a non-inverting amplifier? [1]

Answer _____

(ii) The feedback resistor has a value of 120 kΩ. Which equation could be used to find the value of the other resistor, R, in kΩ, when the voltage gain is 6? (Tick (✓) the correct answer.) [1]

$1 + \left(\frac{120}{R}\right) = 6$ ☐

$1 + \left(\frac{R}{120}\right) = 6$ ☐

$- \left(\frac{120}{R}\right) = 6$ ☐

$- \left(\frac{R}{120}\right) = 6$ ☐

(iii) What is the value of the other resistor, R, in kΩ? [1]

_____

11. **A control system shown opposite is designed to prevent overcrowding in a lift.**

As each person enters the lift, a light beam across the door is broken.

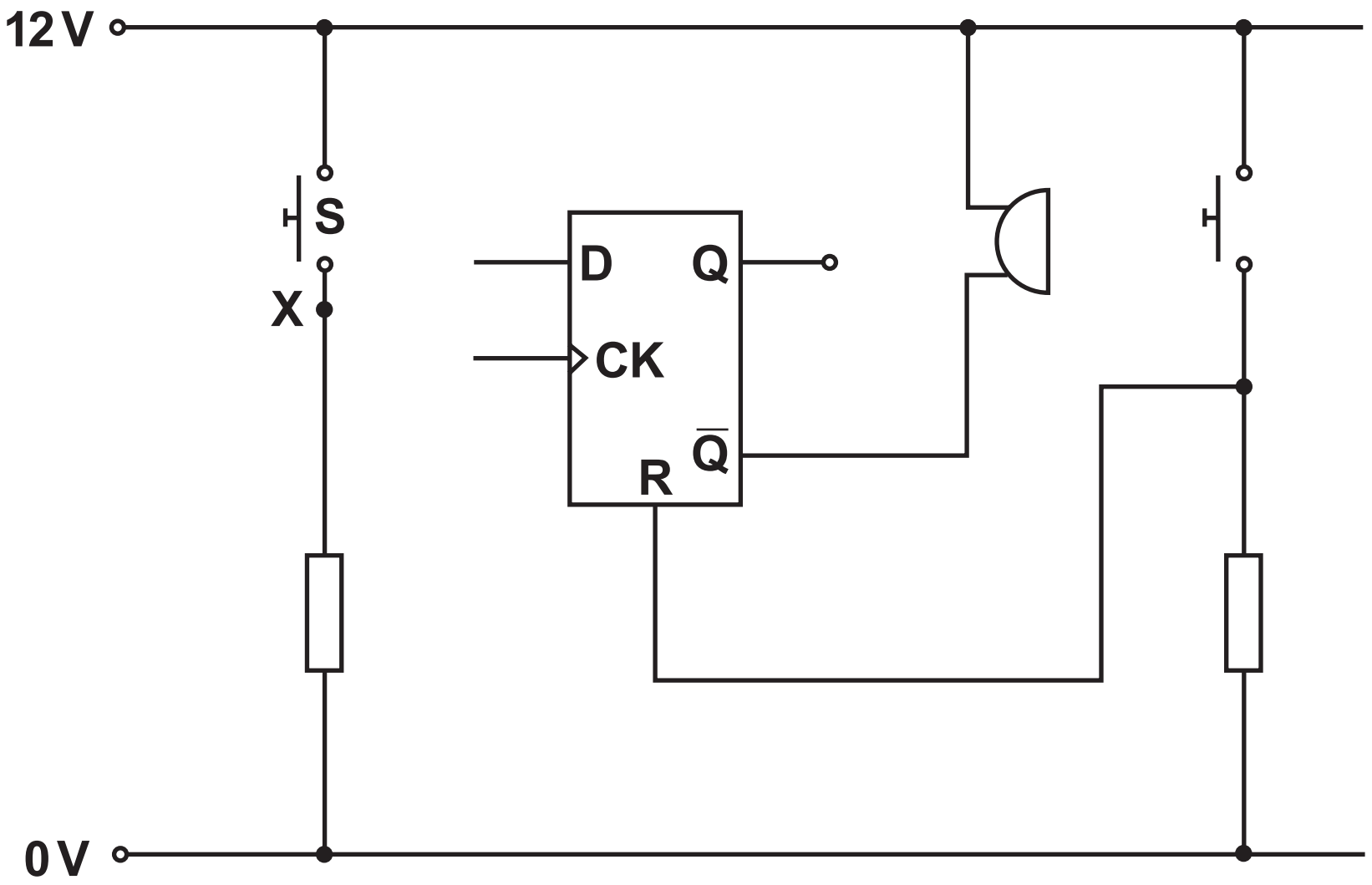
(a) **Explain what is happening between points A and B of the flowchart shown opposite. [2]**

11(b) Explain what is happening between points B and C:

(i) when the count = 5; [1]

(ii) when the count = 11. [1]

(c) Suggest ONE way in which this simple control system could be improved. [1]


12 V
S
X
D
Q
CK
R
$\overline{Q}$
0 V

12. **A rising-edge triggered D-type flip-flop is used as part of a latch circuit as shown opposite.**

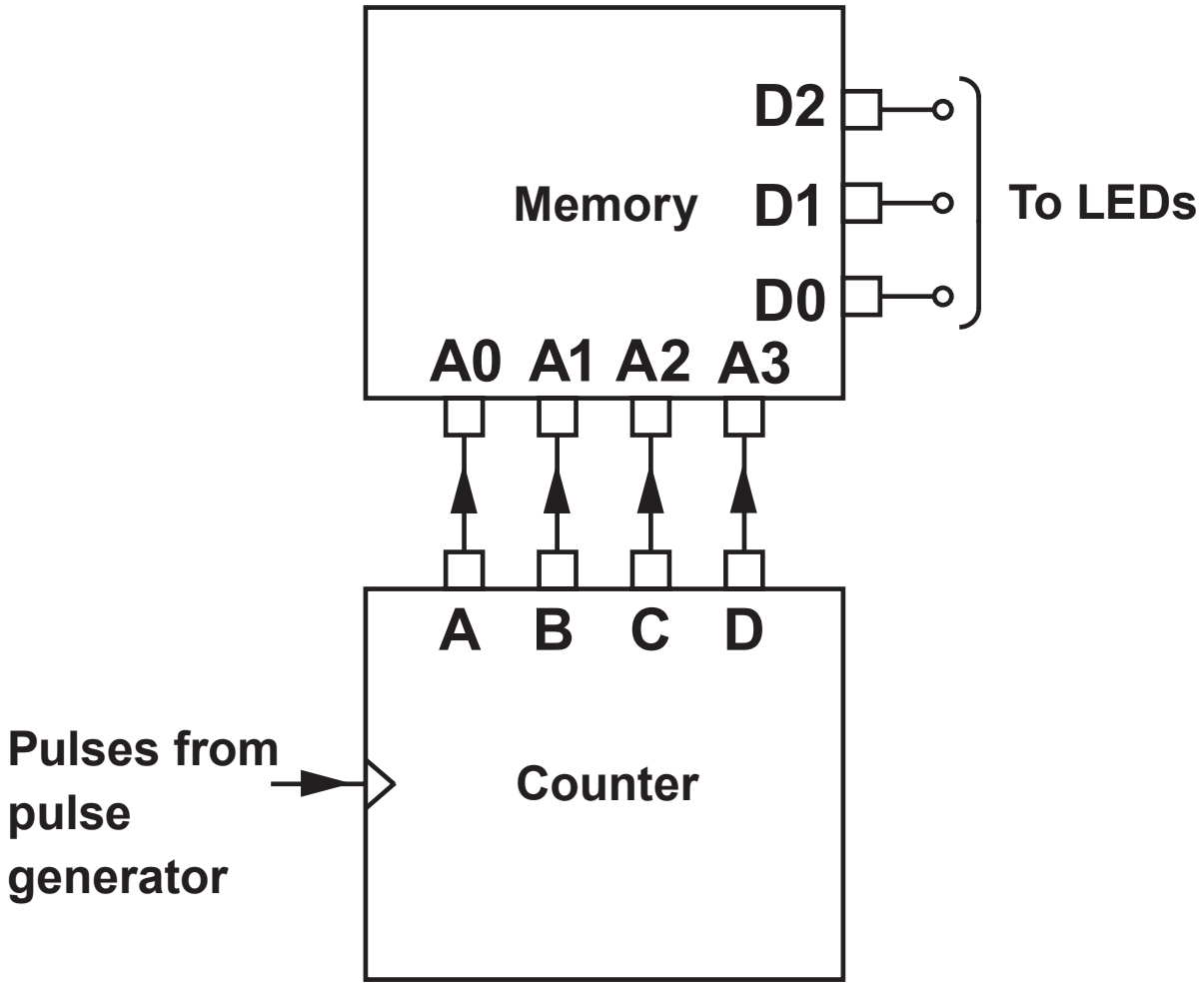
(a) **Select the TWO connections needed to complete the latch.**
(Tick (✓) the correct answers.) [2]

The data input is connected to point X.	☐
The data input is connected to the 0 V power rail.	☐
The data input is connected to the 12 V power rail.	☐
The clock input is connected to point X.	☐
The clock input is connected to the 0 V power rail.	☐
The clock input is connected to the 12 V power rail.	☐

12(b) **Which statement about the correctly configured latch circuit is correct?**
(Tick (✓) the correct answer.) [1]

The buzzer sounds when the $\overline{Q}$ output is at logic 1.	☐
The buzzer sounds when the reset switch is pressed.	☐
Pressing switch S momentarily keeps the buzzer sounding continuously.	☐
Pressing switch S momentarily makes the buzzer beep on and off continuously.	☐

12(c) The upper graph shown opposite shows clock pulses received by a correctly configured latch circuit.
Complete the corresponding **Q** signal. [2]


D2
Memory
D1
To LEDs
D0
A0 A1 A2 A3
A B C D
Pulses from
pulse
generator
Counter

13. **A light sequence controller shown opposite uses a simple memory IC to control some LEDs. The memory IC has four address pins and three data pins.**

(a) **What is the function of the counter in this system? (Tick (✓) the correct answer.) [1]**

It selects memory locations in sequence.	☐
It generates signals to switch the LEDs on and off.	☐
It creates pulses for the pulse generator.	☐
It resets the memory IC after every four pulses from the pulse generator.	☐

13(b) Which of the following statements about the memory IC is true?
(Tick (✓) the correct answer.) [1]

It has 4 memory locations, each storing a 3 bit-number. ☐

It has 4 memory locations, each storing an 8 bit-number. ☐

It has 16 memory locations, each storing a 3 bit-number. ☐

It has 16 memory locations, each storing an 8 bit-number. ☐

14(a) A control system for automatic car headlamps is shown below.

Part of the data sheet for the Schmitt inverter is shown below.

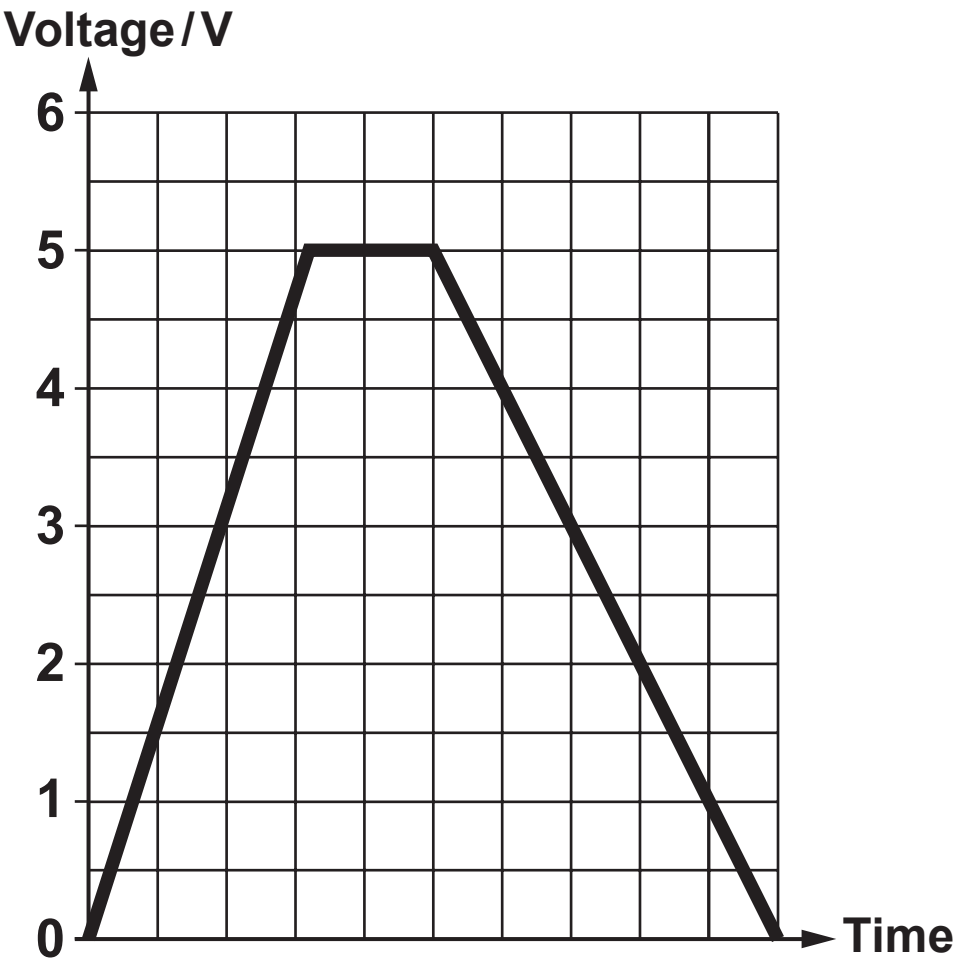
When connected to a 12 V car battery:

- **Logic 0 = 0 V;**
- **Logic 1 = 12 V;**
- **The output changes from logic 1 to logic 0 when a RISING input voltage reaches 8 V;**
- **The output changes from logic 0 to logic 1 when a FALLING input voltage reaches 4 V.**

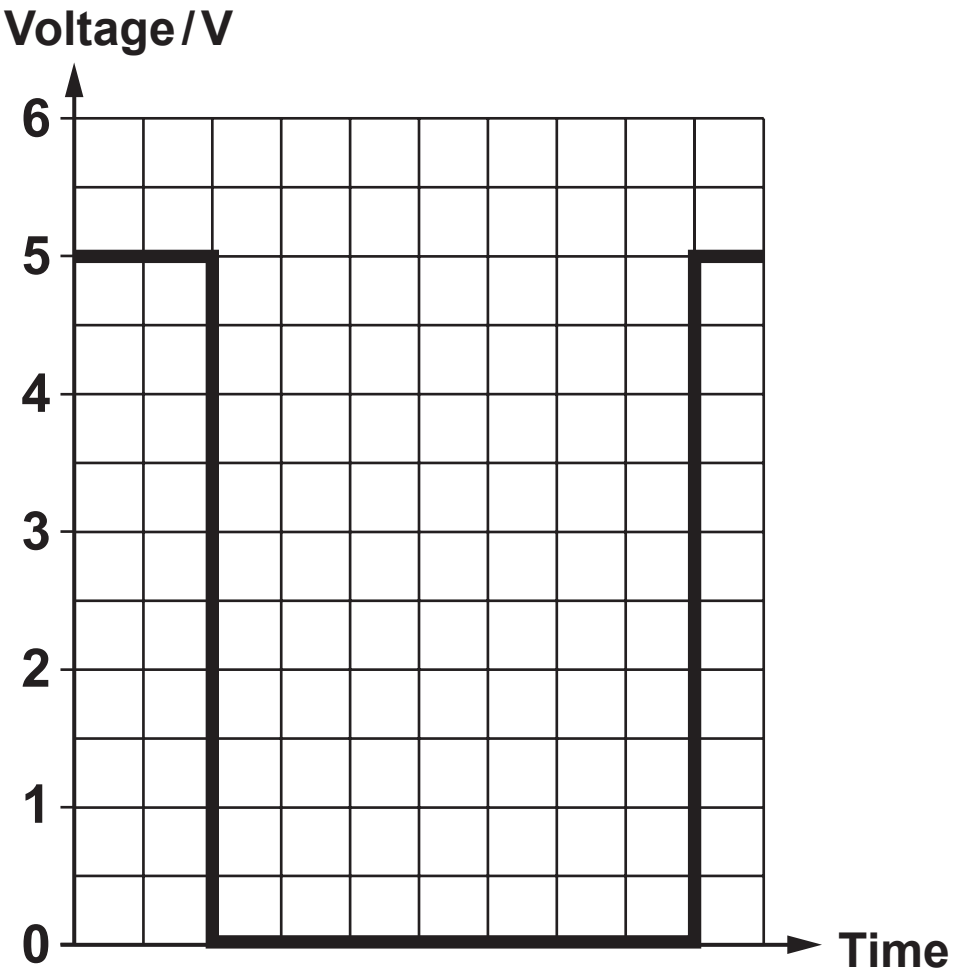
14(a) The light sensing unit output signal is shown opposite in the top graph.

Draw the output signal of the Schmitt inverter on the bottom graph. [3]

Input voltage,
V_{IN}



Output voltage,
V_{OUT}



14(b) **The graphs opposite show the input and output signals for a DIFFERENT Schmitt inverter.**

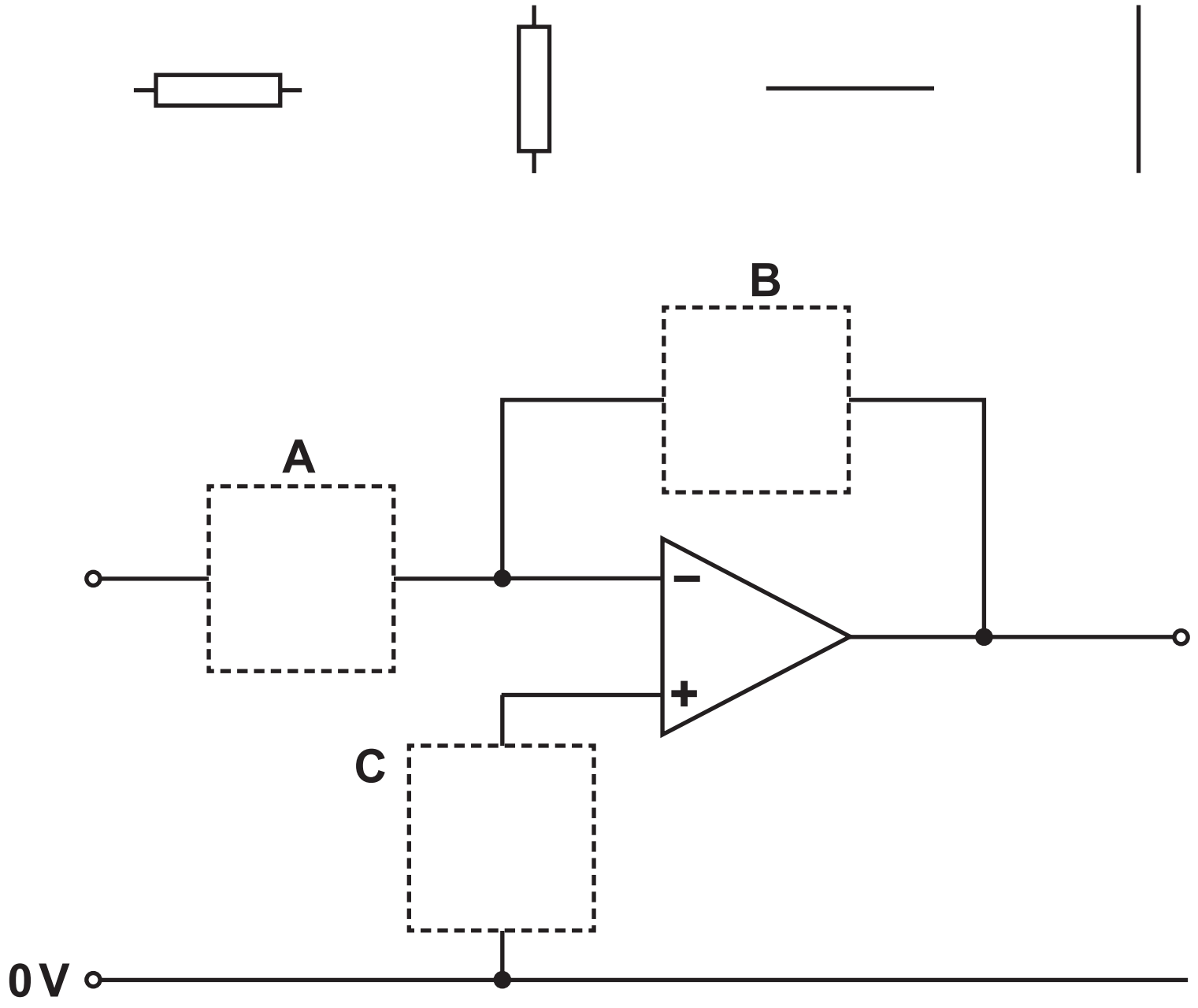
Complete the following sentences.

(i) **The output of the Schmitt inverter changes from 5 V to 0 V when a RISING input**

voltage reaches _____ V. [1]

(ii) **The output of the Schmitt inverter changes from 0 V to 5 V when a FALLING input**

voltage reaches _____ V. [1]

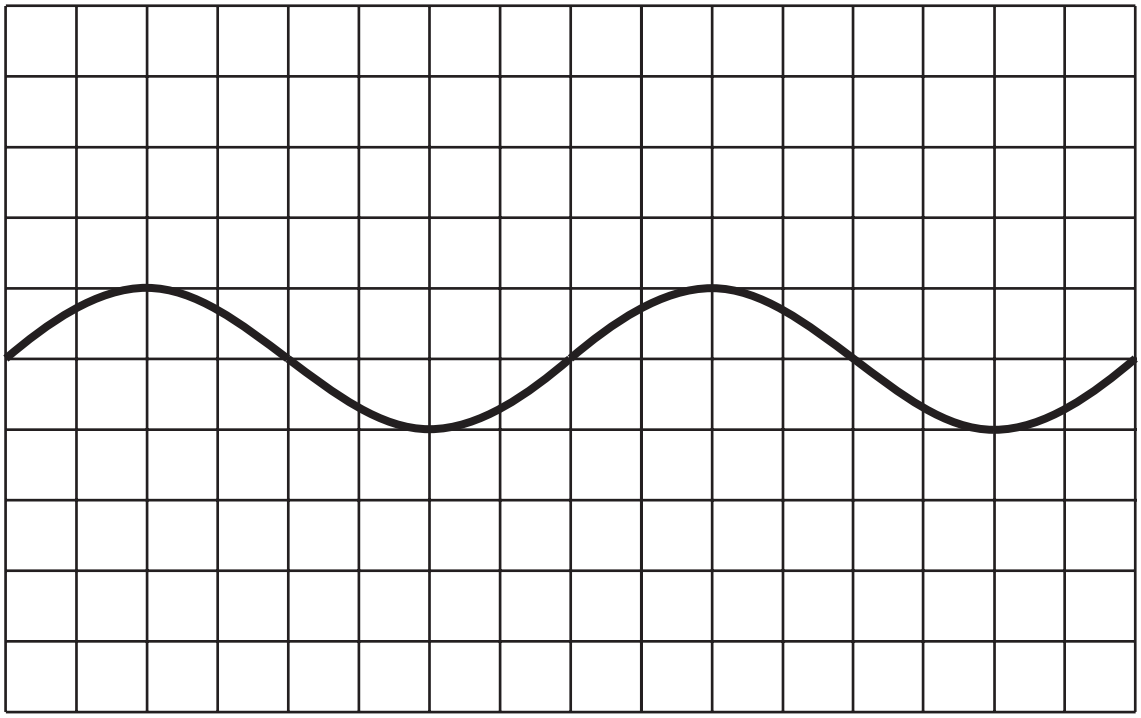

B
A
−
+
C
0 V

15(a) A project requires an inverting amplifier with a voltage gain of **–13**.

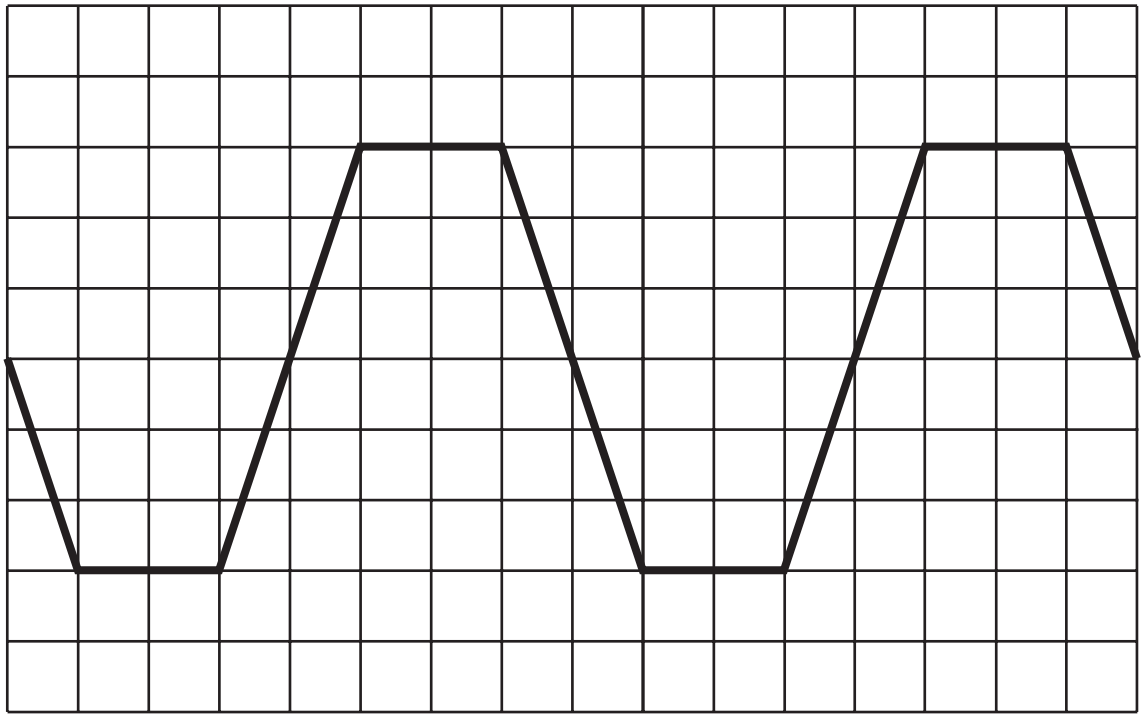
(i) Draw the correct components to complete the circuit diagram opposite. [3]

(ii) Select the combination of feedback and input resistors that will produce a voltage gain of **–13**. (Tick (✓) the correct answer.) [1]

Feedback resistor	Input resistor	
10 kΩ	130 kΩ	
10 kΩ	120 kΩ	
130 kΩ	10 kΩ	
120 kΩ	10 kΩ	



Input signal



Output signal

15(b) **The input and output signals are viewed on an oscilloscope. The traces are shown opposite.**

The output signal is distorted.

(i) **What is this distortion called? [1]**

_____

_____

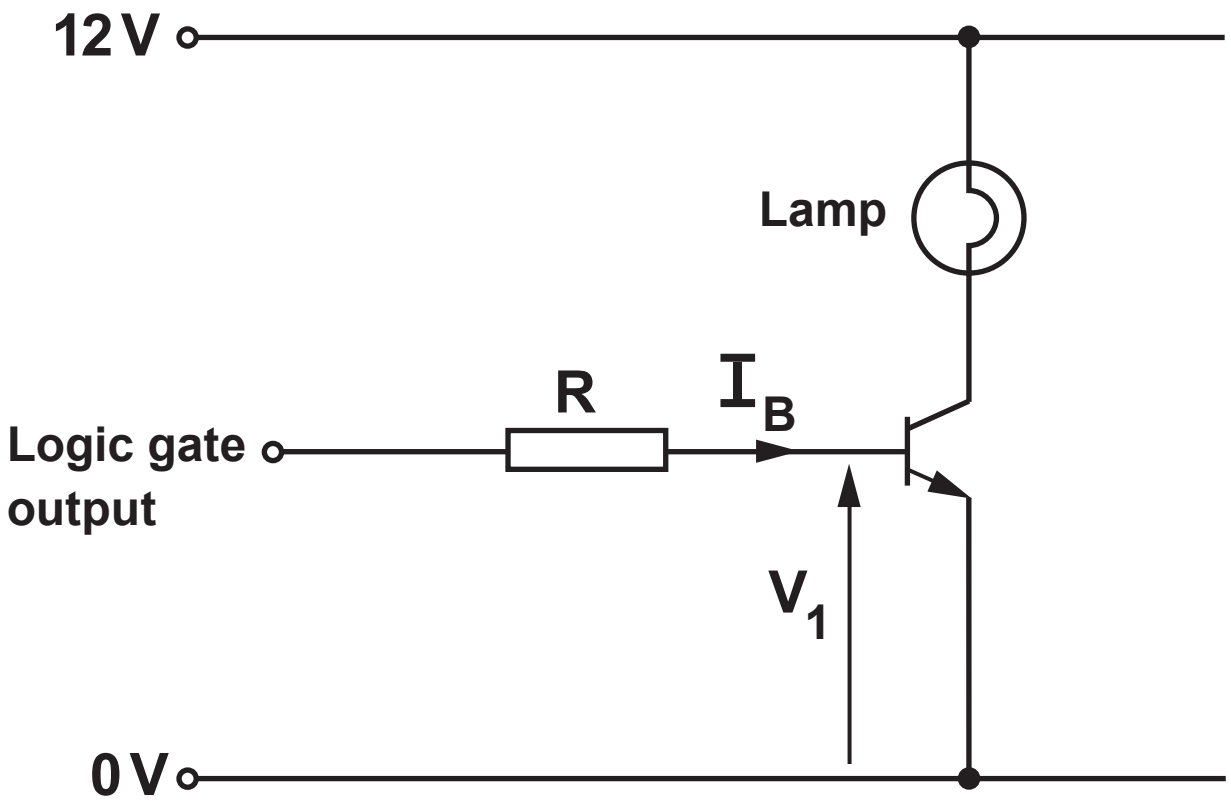
(ii) **Describe ONE way of eliminating it. [1]**

_____

_____

_____

_____


12 V
Lamp
R
I_B
Logic gate output
V_1
0 V

16. The diagram opposite shows a transistor used to interface a logic gate to a lamp. The lamp lights fully when the logic gate outputs a logic 1 signal (which is $8.7\,V$). At this point the transistor is just saturated.

When fully lit, the current through the lamp = $80\,mA$.

The current gain, h_{FE} of the transistor = 40.

(a) Calculate the base current, I_B. [1]

I_B = _____ mA

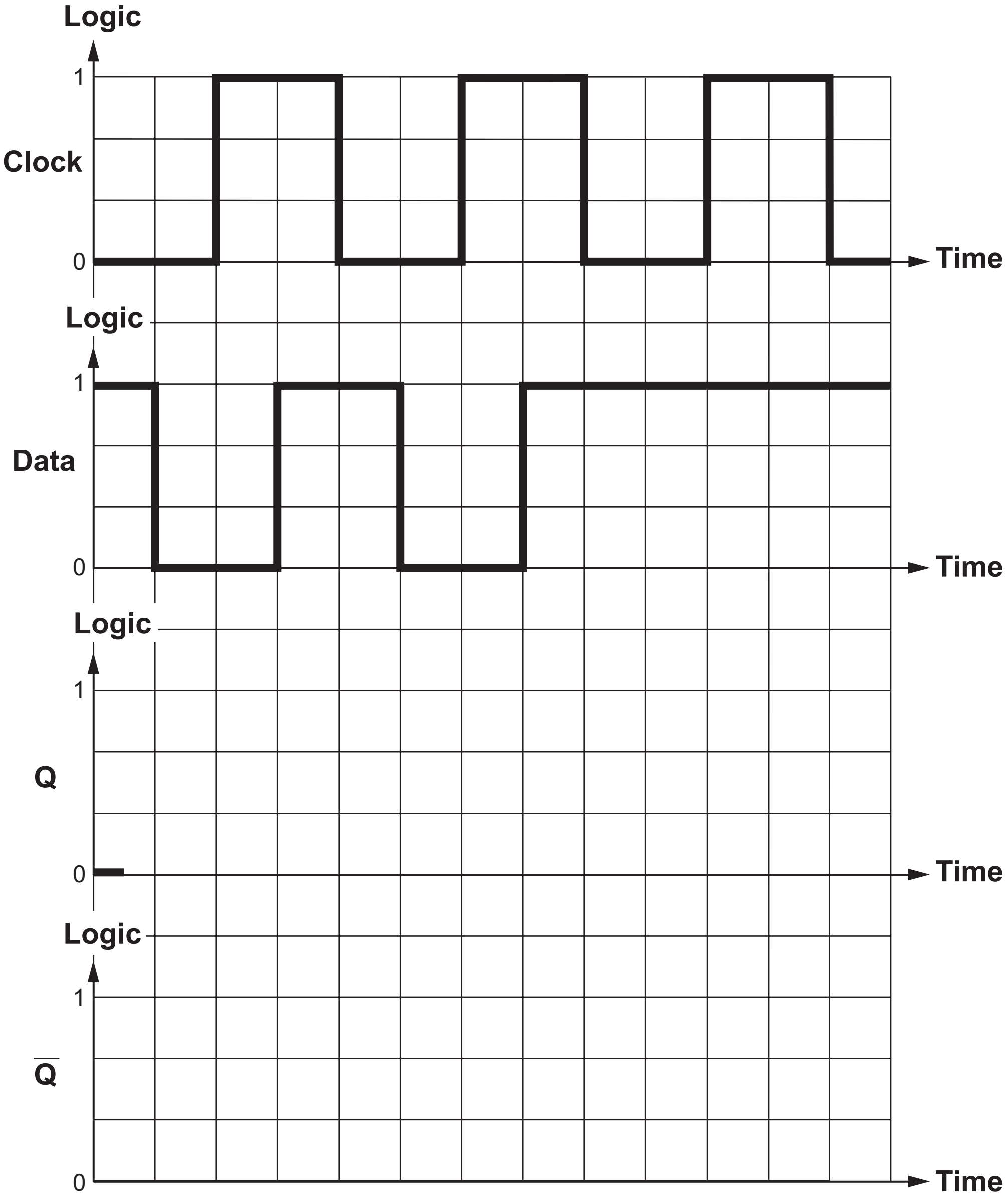
16(b) The logic gate outputs 8.7 V. What is the voltage drop across resistor R? [1]

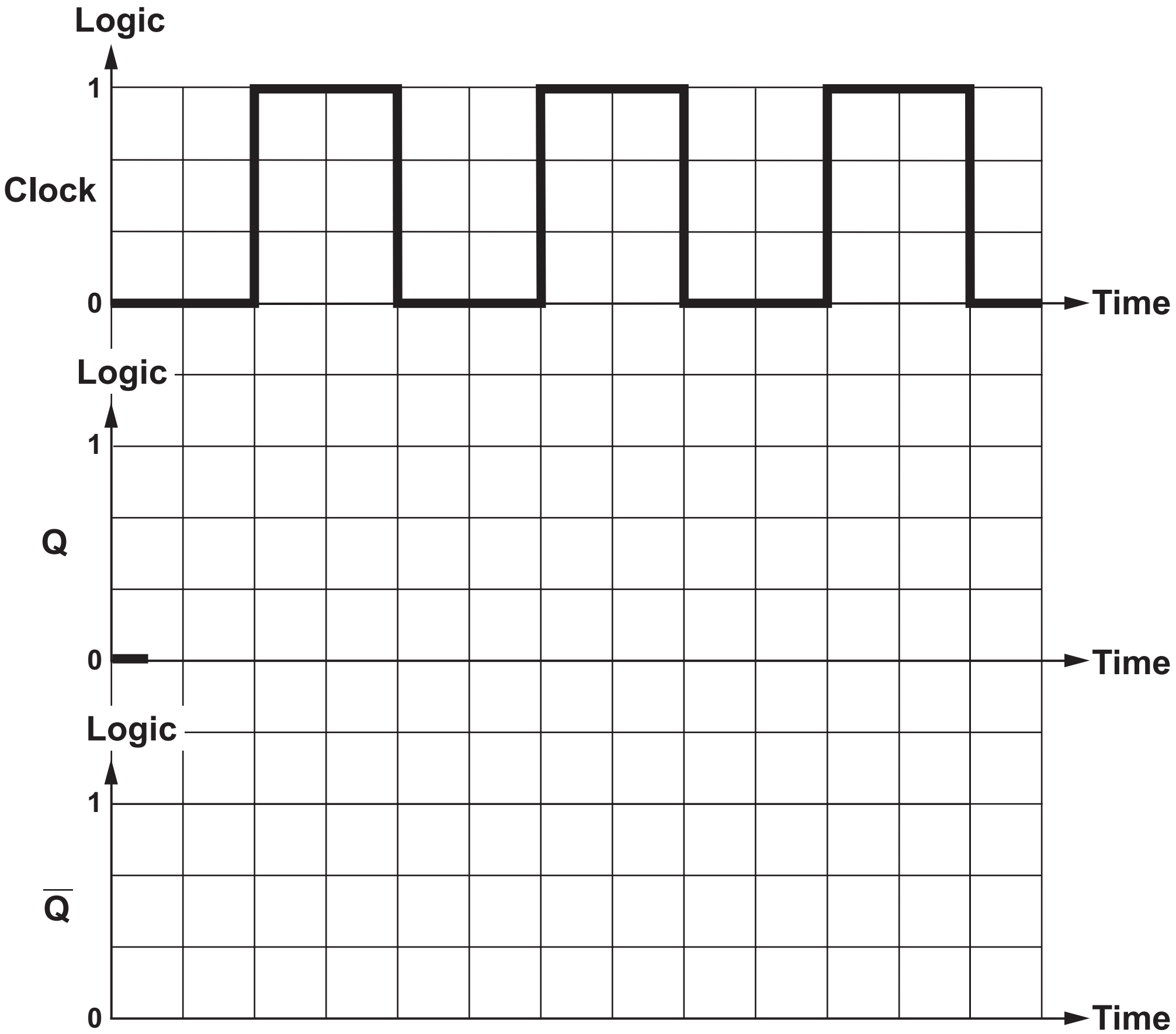
Voltage drop = _____ V

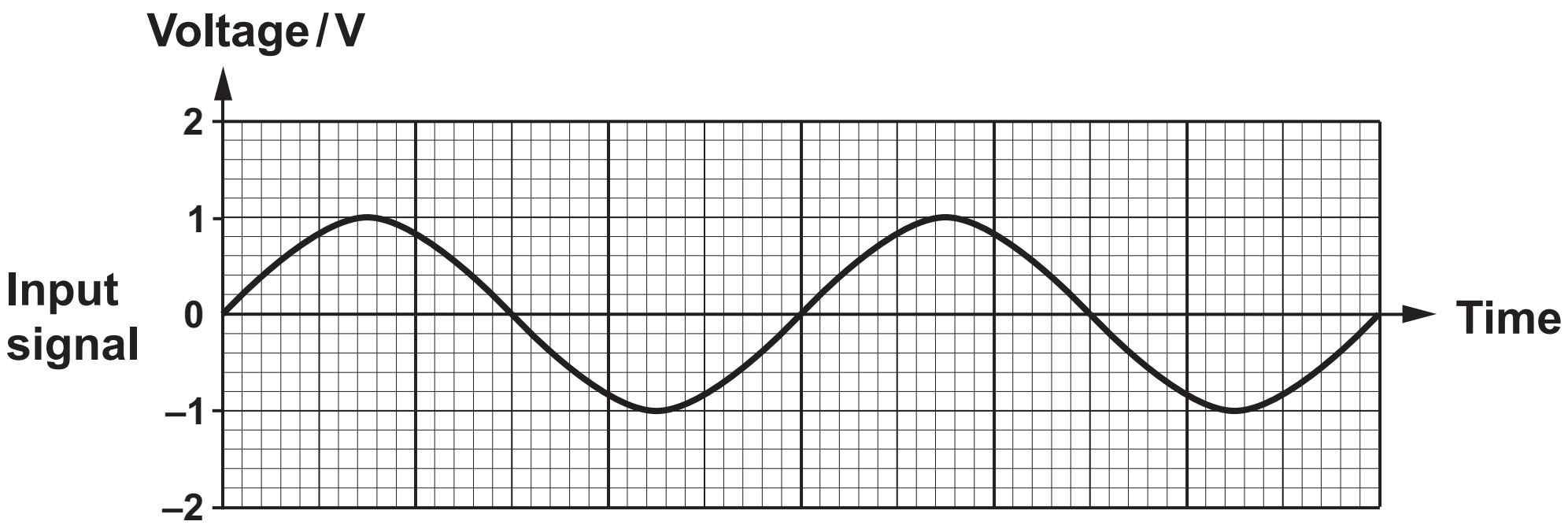
(c) Hence calculate the value of resistor R. [1]

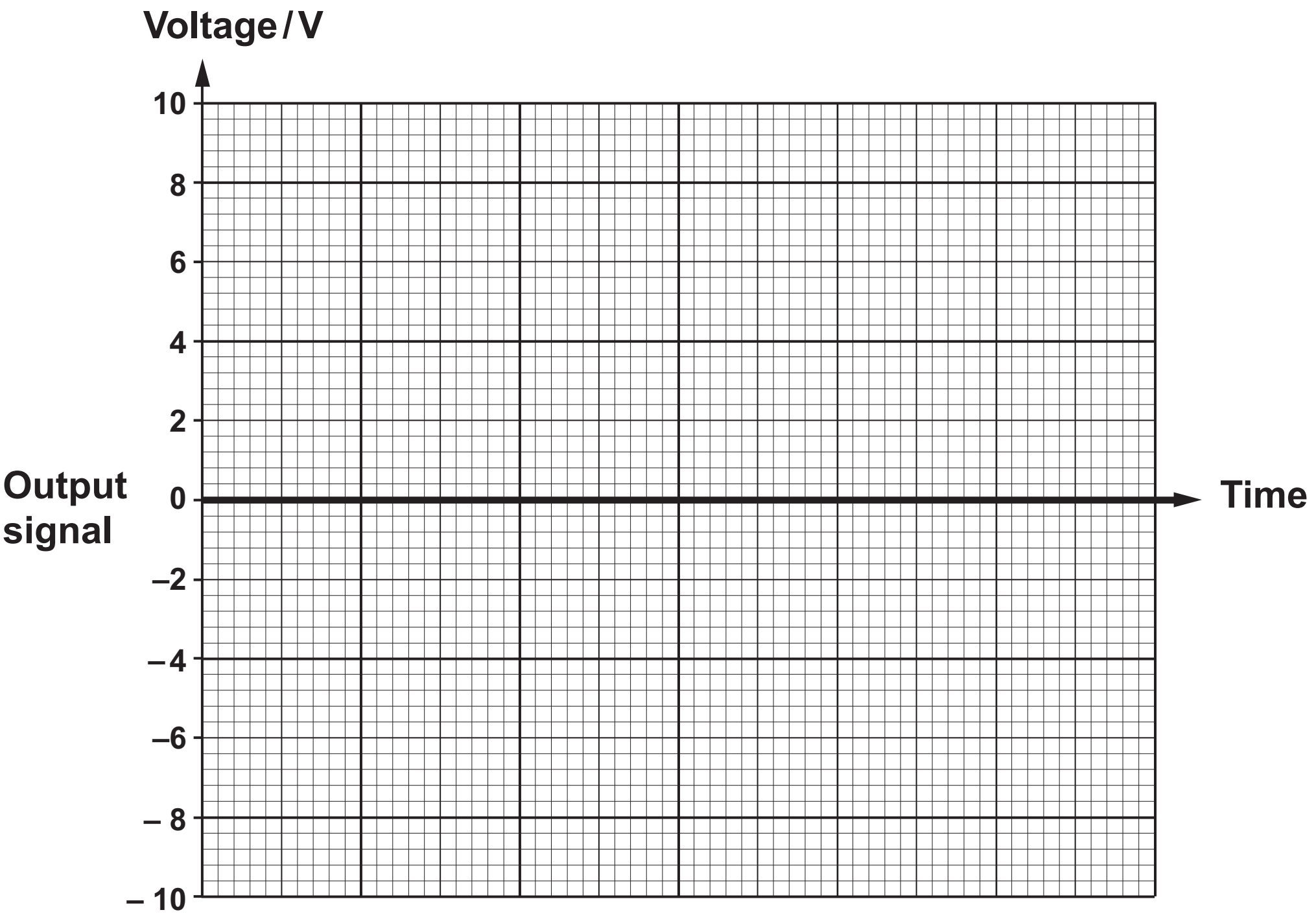
R = _____ kΩ

END OF PAPER

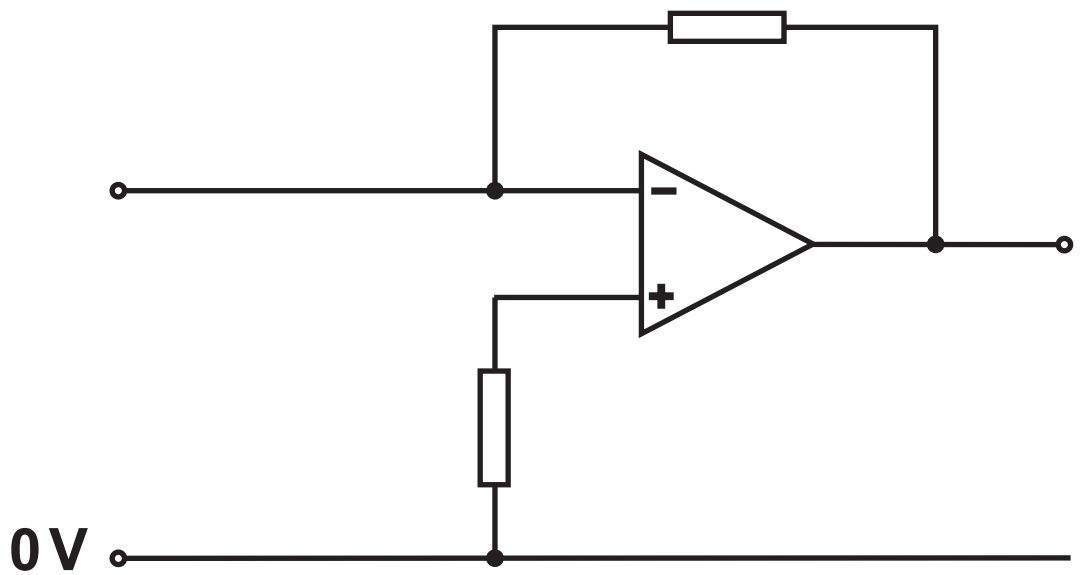

Logic
1
Clock
0
Time
Logic
1
Data
0
Time
Logic
1
Q
0
Time
Logic
1
$\overline{Q}$
0
Time


Logic
1
Clock
0
Time
Logic
1
Q
0
Time
Logic
1
$\overline{Q}$
0
Time

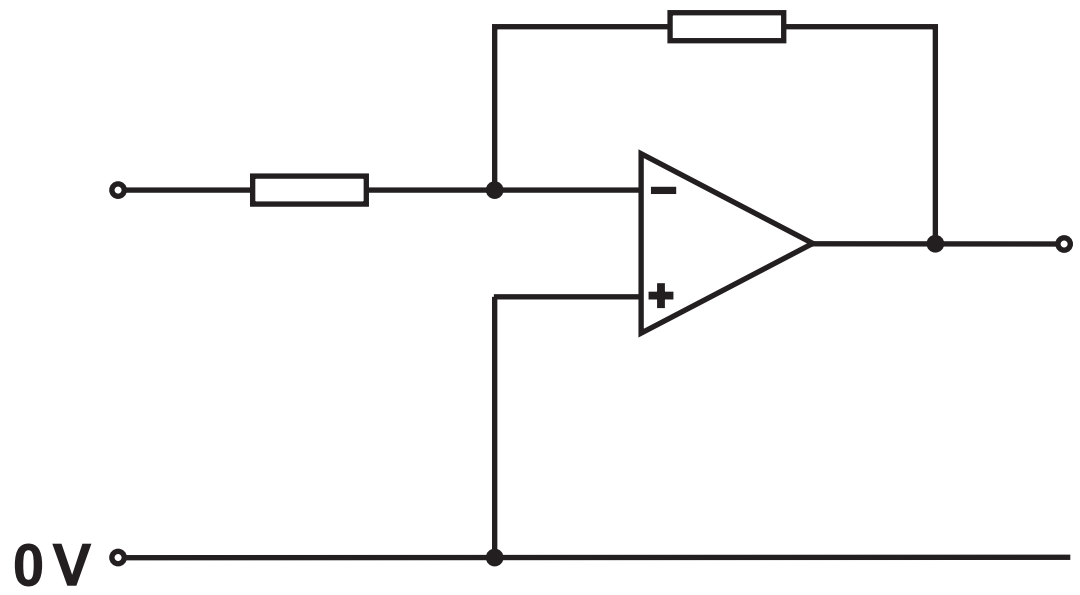

Voltage / V
2
1
0
–1
–2
Input signal
Time


Voltage / V
10
8
6
4
2
0
–2
–4
–6
– 8
– 10
Output signal
Time

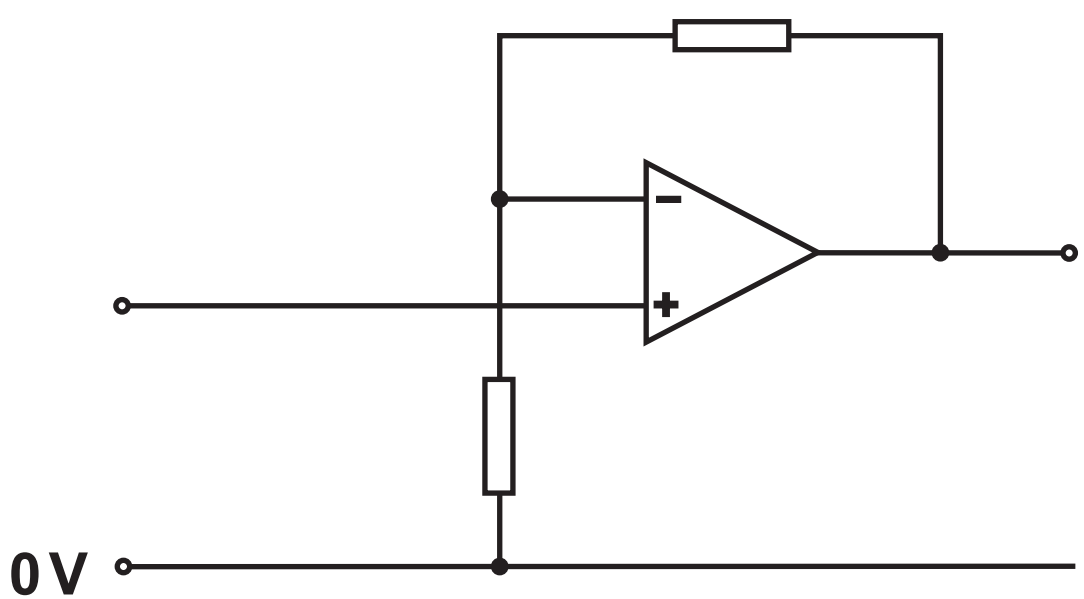
A



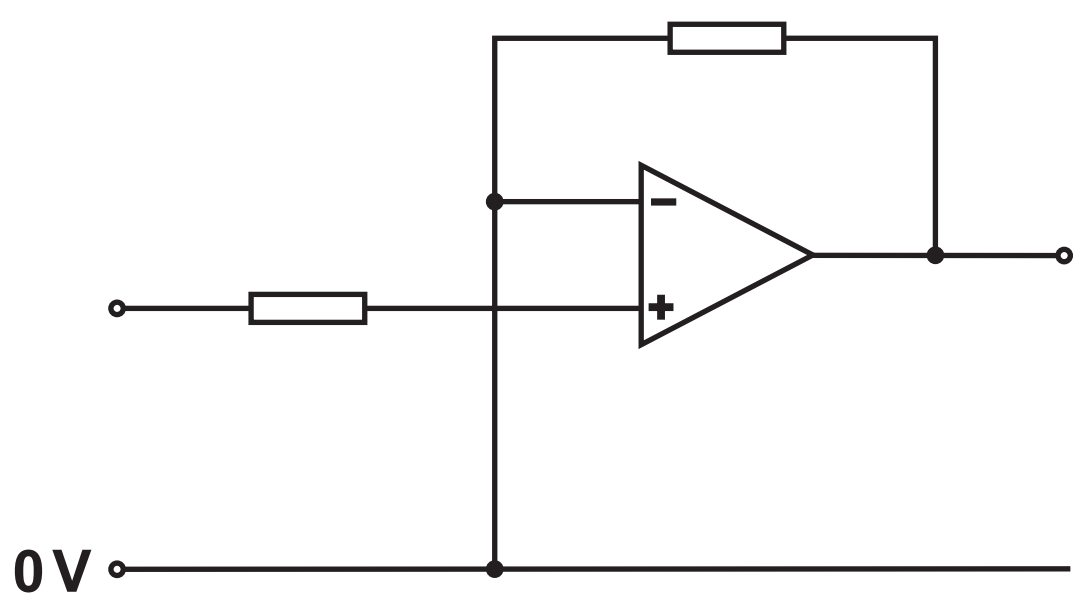
B

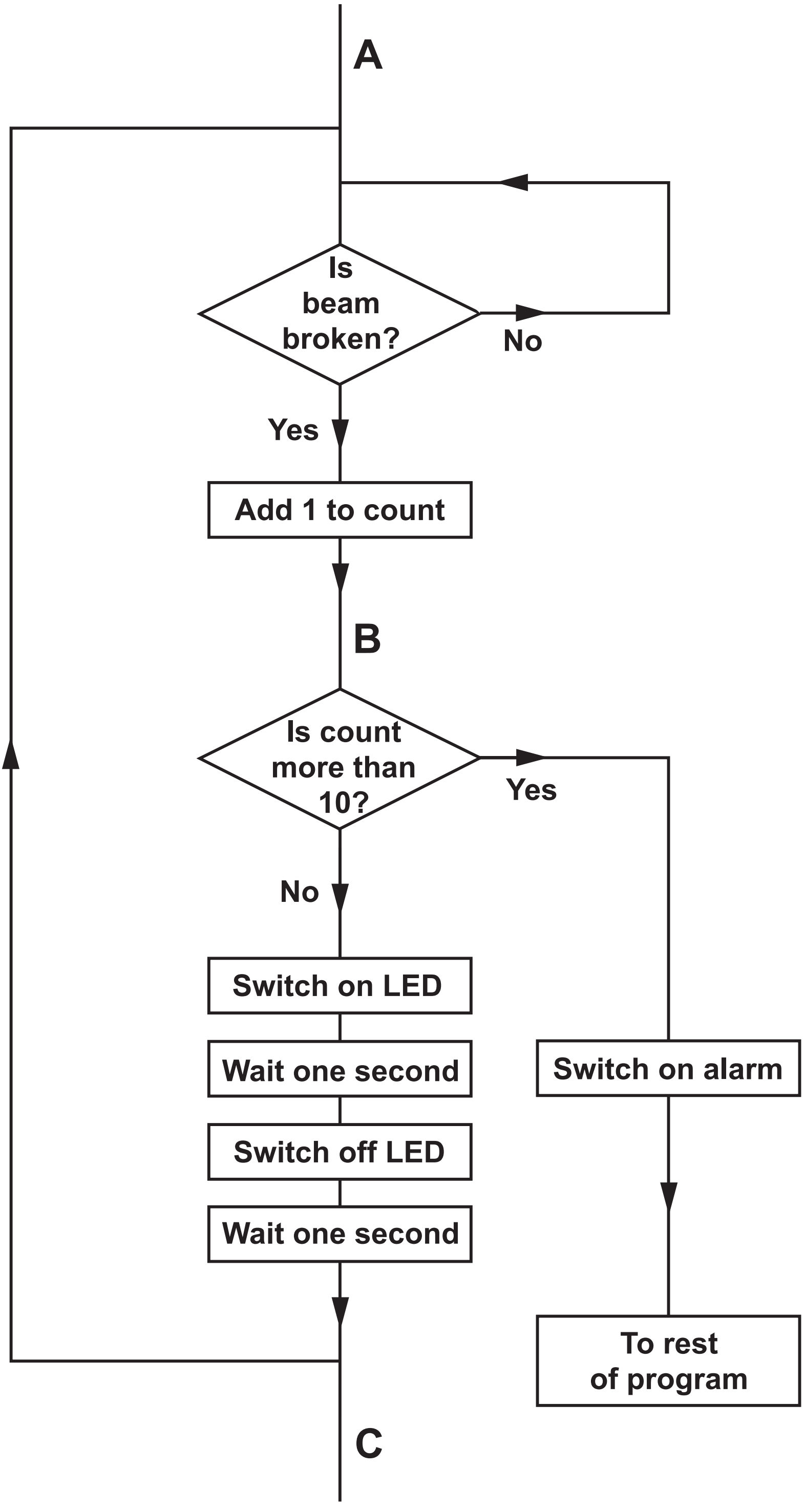


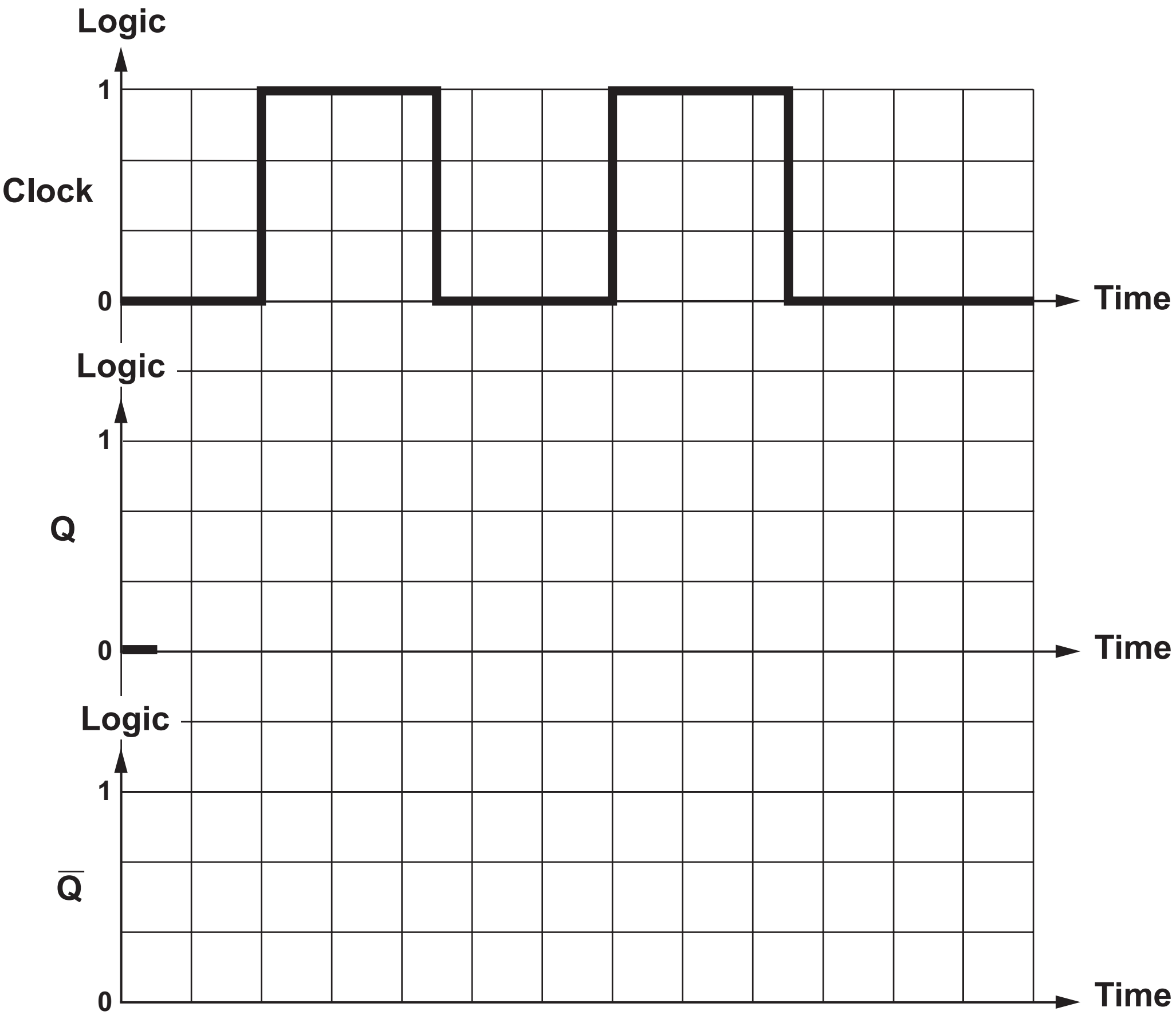
C



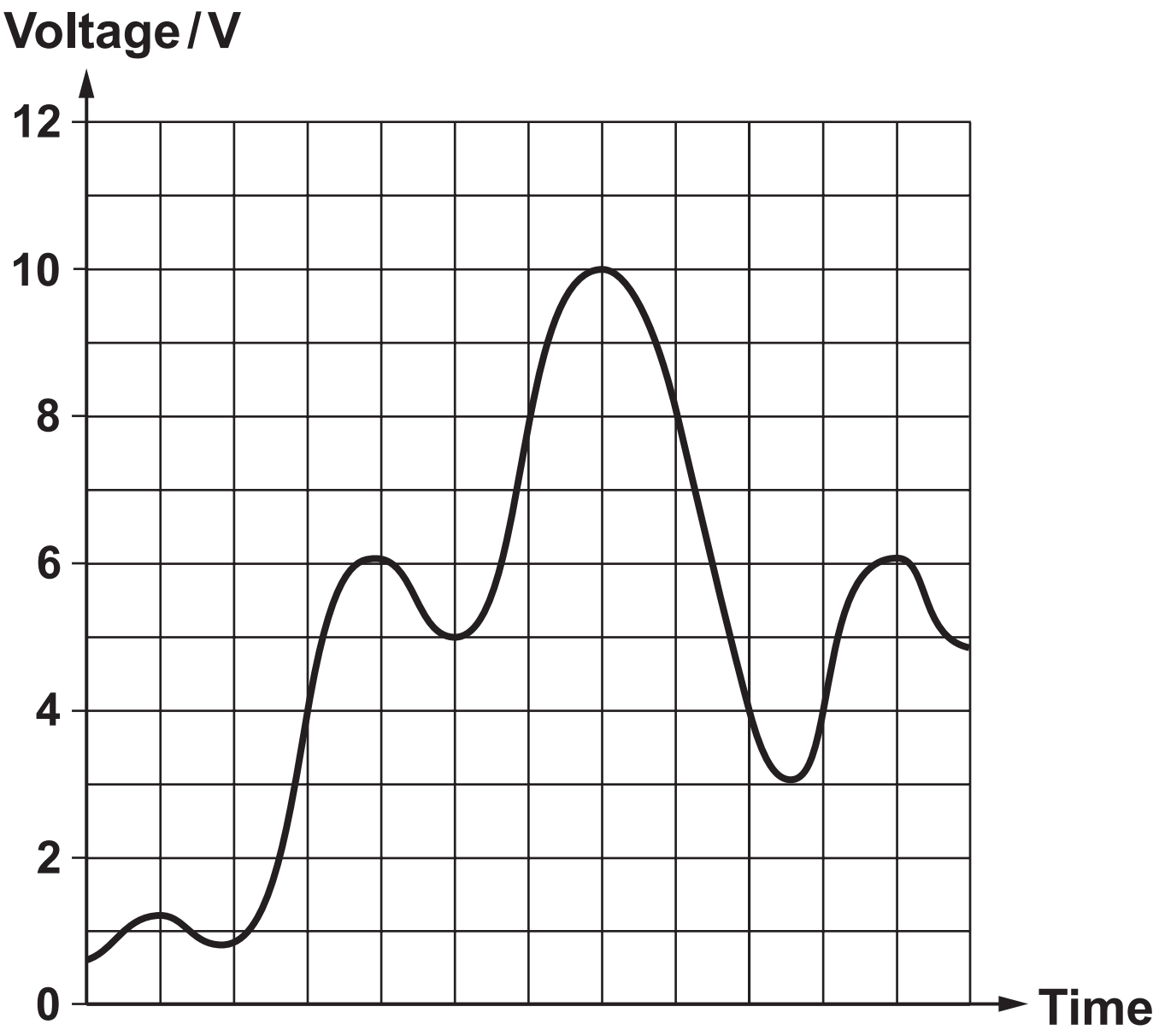
D




A
Is beam broken?
No
Yes
Add 1 to count
B
Is count more than 10?
Yes
No
Switch on LED
Wait one second
Switch off LED
Wait one second
Switch on alarm
To rest of program
C


Logic
1
Clock
0
Time
Logic
1
Q
0
Time
Logic
1
$\overline{Q}$
0
Time

Output of light sensing unit



Output of Schmitt inverter